US009425272B2

(12) **United States Patent**
**Becker et al.**

(10) **Patent No.: US 9,425,272 B2**
(45) **Date of Patent: *Aug. 23, 2016**

(54) **SEMICONDUCTOR CHIP INCLUDING INTEGRATED CIRCUIT INCLUDING FOUR TRANSISTORS OF FIRST TRANSISTOR TYPE AND FOUR TRANSISTORS OF SECOND TRANSISTOR TYPE WITH ELECTRICAL CONNECTIONS BETWEEN VARIOUS TRANSISTORS AND METHODS FOR MANUFACTURING THE SAME**

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( * ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **14/731,316**

(22) Filed: **Jun. 4, 2015**

(65) **Prior Publication Data**

US 2015/0270218 A1 Sep. 24, 2015

**Related U.S. Application Data**

(63) Continuation of application No. 13/774,919, filed on Feb. 22, 2013, which is a continuation of application No. 12/572,225, filed on Oct. 1, 2009, now Pat. No. 8,436,400, which is a continuation of application No.

(Continued)

(51) **Int. Cl.**
***H01L 27/10*** (2006.01)
***H01L 29/423*** (2006.01)

(Continued)

(52) **U.S. Cl.**
CPC ..... ***H01L 29/42376*** (2013.01); ***G06F 17/5068*** (2013.01); ***G06F 17/5072*** (2013.01);

(Continued)

(58) **Field of Classification Search**
CPC ..... H01L 27/027; H01L 27/11807; H01L 27/1104; H01L 27/11; H01L 27/092
USPC ..... 257/202, 204, 206, 211, 365
See application file for complete search history.

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U.S. Appl. No. 60/625,342, Pileggi et al., filed May 25, 2006.

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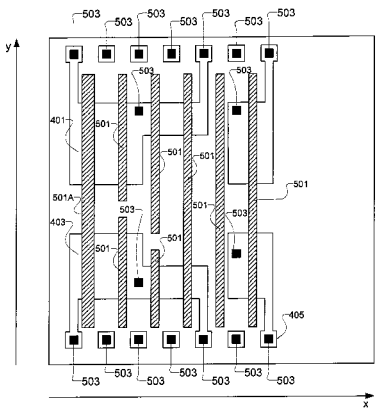
(57) **ABSTRACT**

A semiconductor chip region includes a first conductive structure (CS) that forms a gate electrode (GE) of a first transistor of a first transistor type (TT) and a GE of a first transistor of a second TT, a second CS that forms a GE of a second transistor of the first TT, a third CS that forms a GE of a second transistor of the second TT, a fourth CS that forms a GE of a third transistor of the first TT, a fifth CS that forms a GE of a third transistor of the second TT, another CS that forms a GE of a fourth transistor of the first TT, and another CS that forms a GE of a fourth transistor of the second TT. The second and third transistors of the first and second TT's have a common diffusion terminal electrical connection and specified gate electrode electrical connections.

**30 Claims, 28 Drawing Sheets**



**Related U.S. Application Data**

12/212,562, filed on Sep. 17, 2008, now Pat. No. 7,842,975, which is a continuation of application No. 11/683,402, filed on Mar. 7, 2007, now Pat. No. 7,446,352.

(60) Provisional application No. 60/781,288, filed on Mar. 9, 2006.

(51) **Int. Cl.**

| | |
|---|---|
| ***H01L 27/092*** | (2006.01) |
| ***H01L 27/02*** | (2006.01) |
| ***G06F 17/50*** | (2006.01) |
| ***H01L 27/088*** | (2006.01) |
| ***H01L 21/8238*** | (2006.01) |
| ***H01L 27/118*** | (2006.01) |
| ***H01L 23/522*** | (2006.01) |
| ***H01L 23/528*** | (2006.01) |

(52) **U.S. Cl.**

CPC .... ***H01L21/823871*** (2013.01); ***H01L 23/5226*** (2013.01); ***H01L 23/5283*** (2013.01); ***H01L 27/0207*** (2013.01); ***H01L 27/088*** (2013.01); ***H01L 27/092*** (2013.01); ***H01L 27/11807*** (2013.01); ***H01L 29/42372*** (2013.01); *H01L 2027/11888* (2013.01); *H01L 2924/0002* (2013.01)

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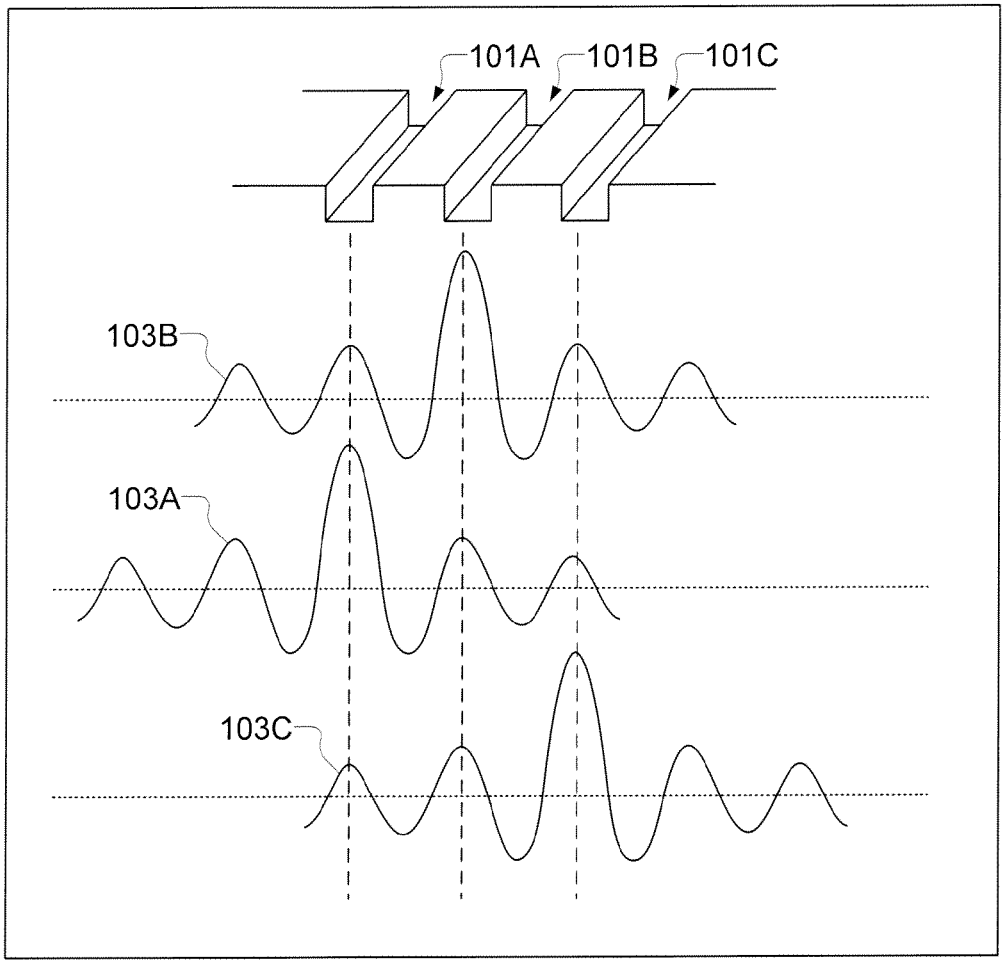



Fig. 1

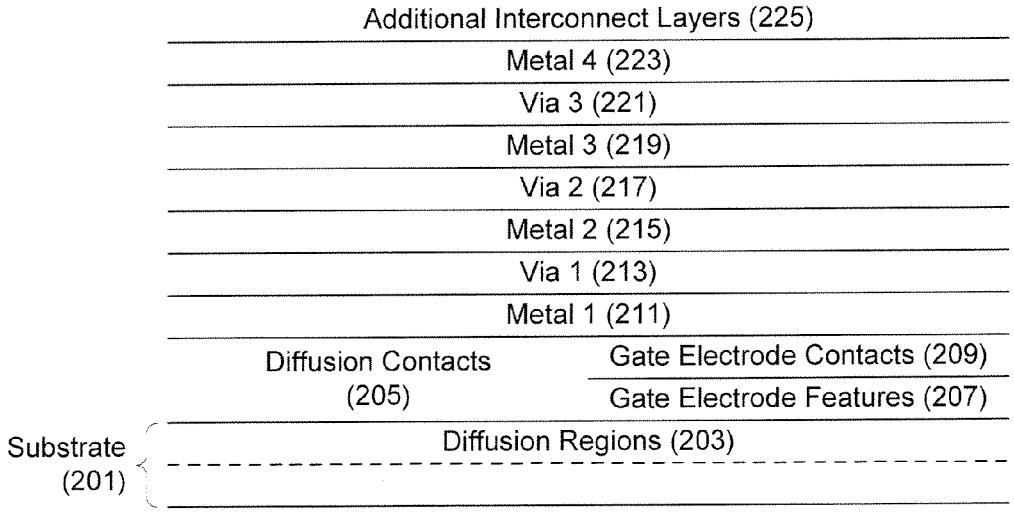

Additional Interconnect Layers (225)
Metal 4 (223)
Via 3 (221)
Metal 3 (219)
Via 2 (217)
Metal 2 (215)
Via 1 (213)
Metal 1 (211)
Diffusion Contacts (205)
Gate Electrode Contacts (209)
Gate Electrode Features (207)
Diffusion Regions (203)
Substrate (201)

Fig. 2

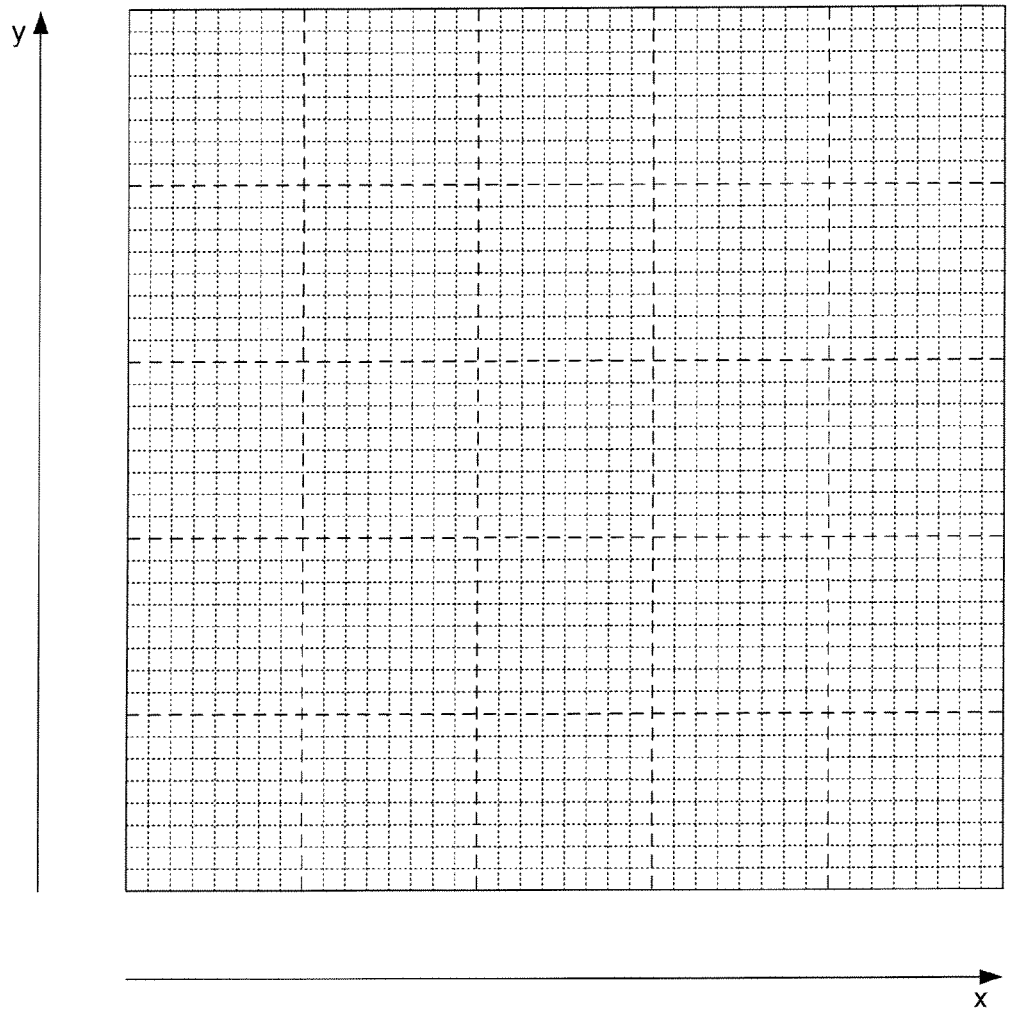



Fig. 3A

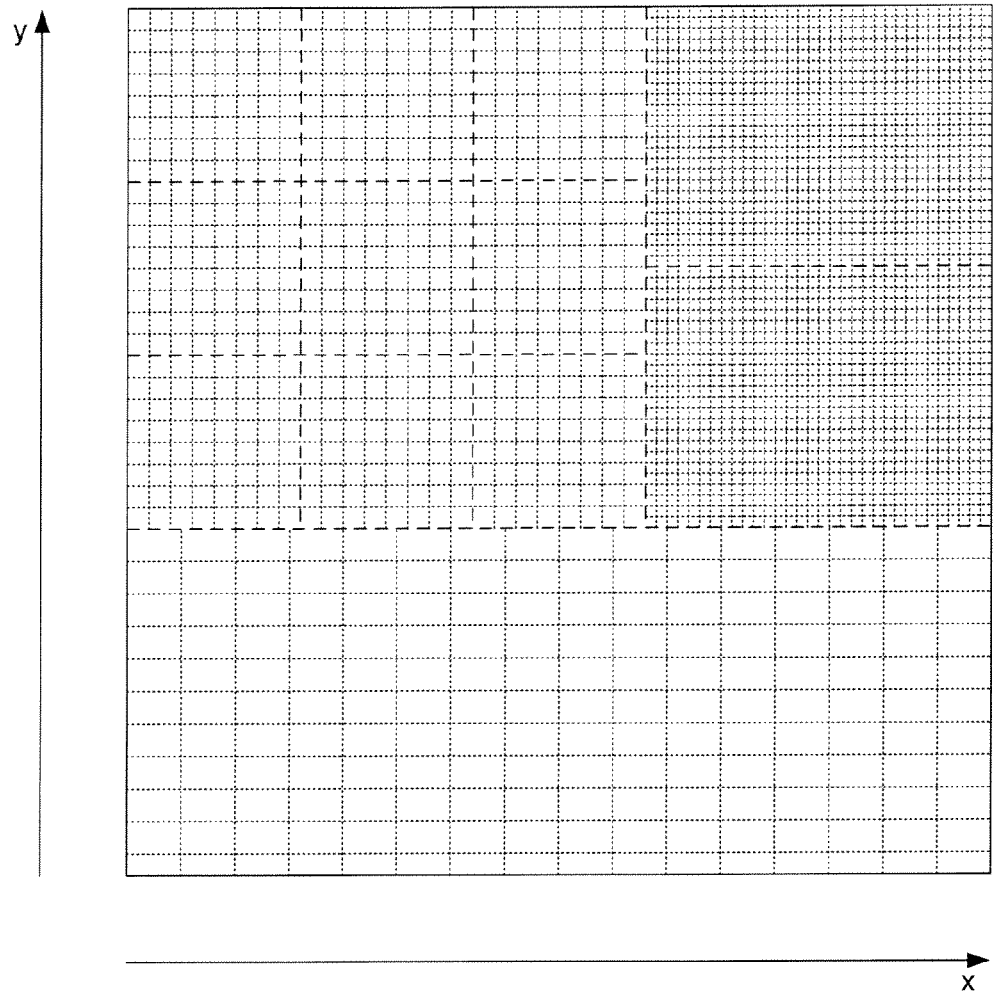



Fig. 3B

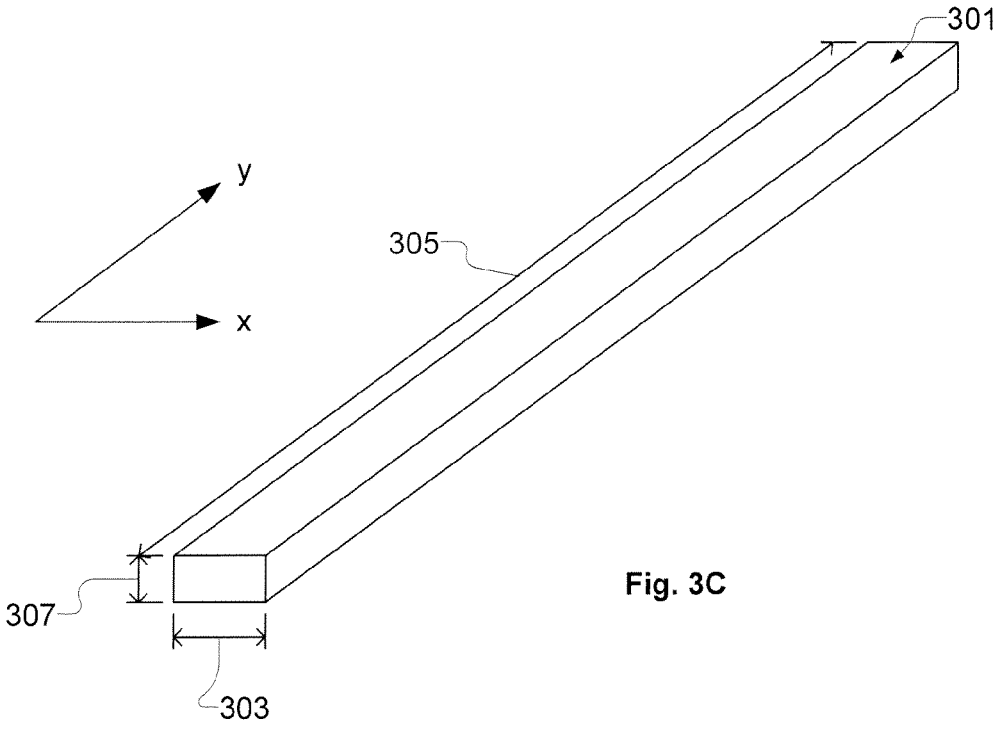



Fig. 3C

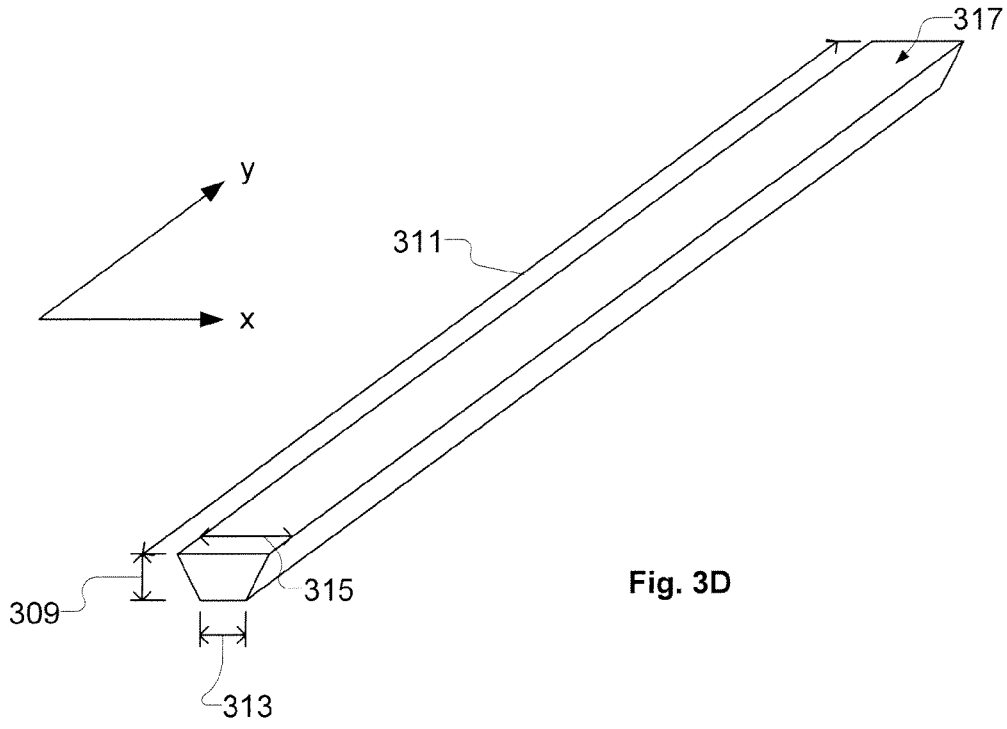



Fig. 3D

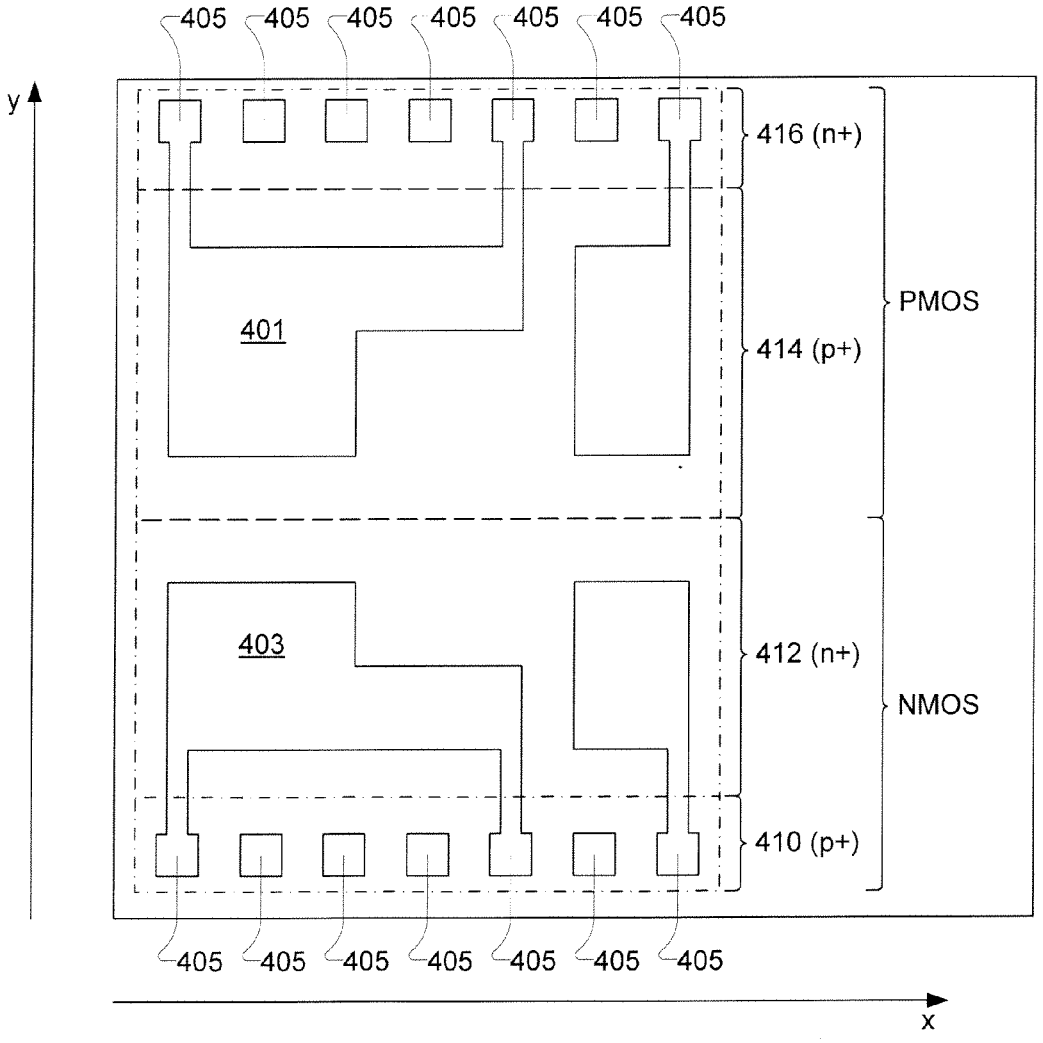

405
405
405
405
405
405
405
y
416 (n+)
401
414 (p+)
PMOS
403
412 (n+)
NMOS
410 (p+)
405
405
405
405
405
405
405
x

Fig. 4

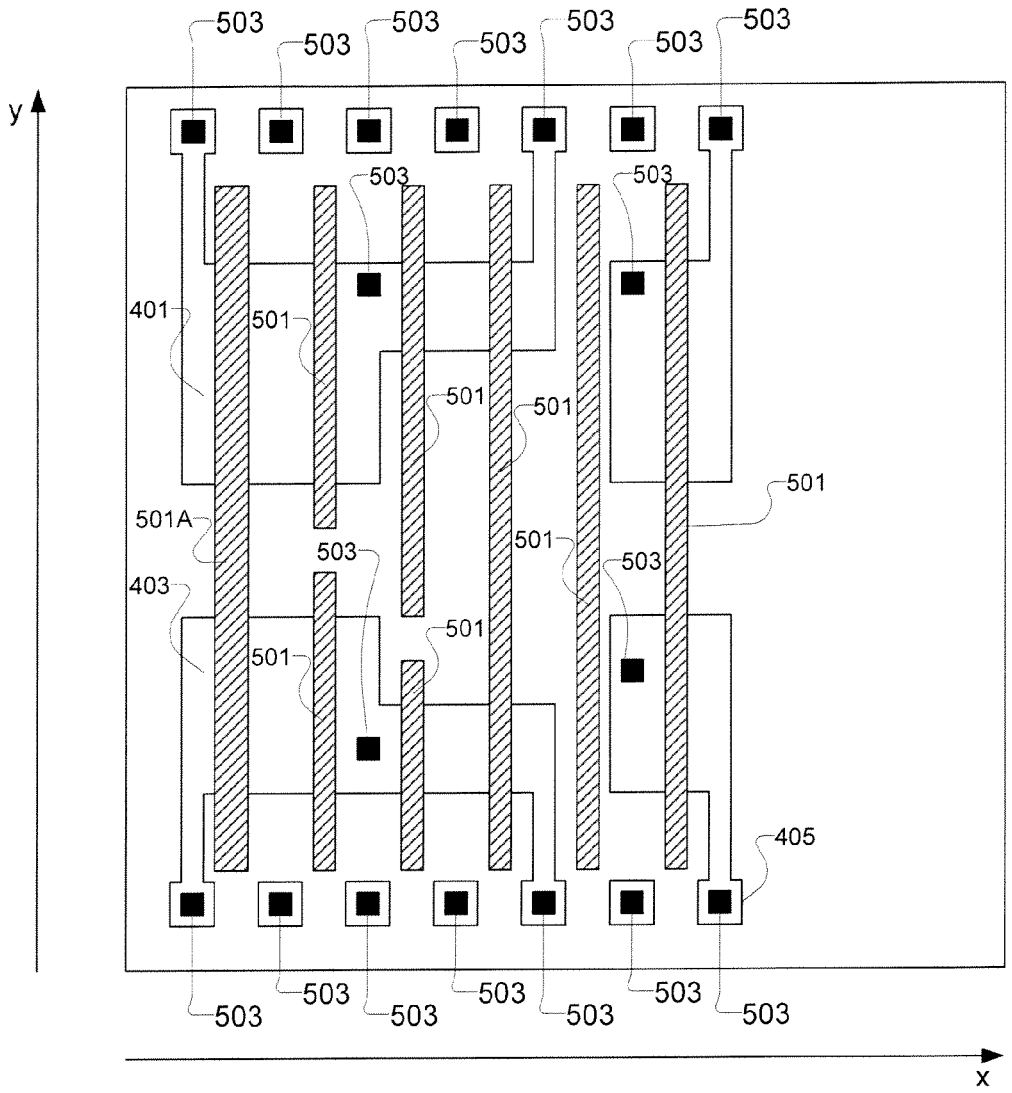

503
503
503
503
503
503
503
y
503
503
401
501
501
501
501
501A
503
503
403
501
501
405
503
503
503
503
503
503
x

Fig. 5

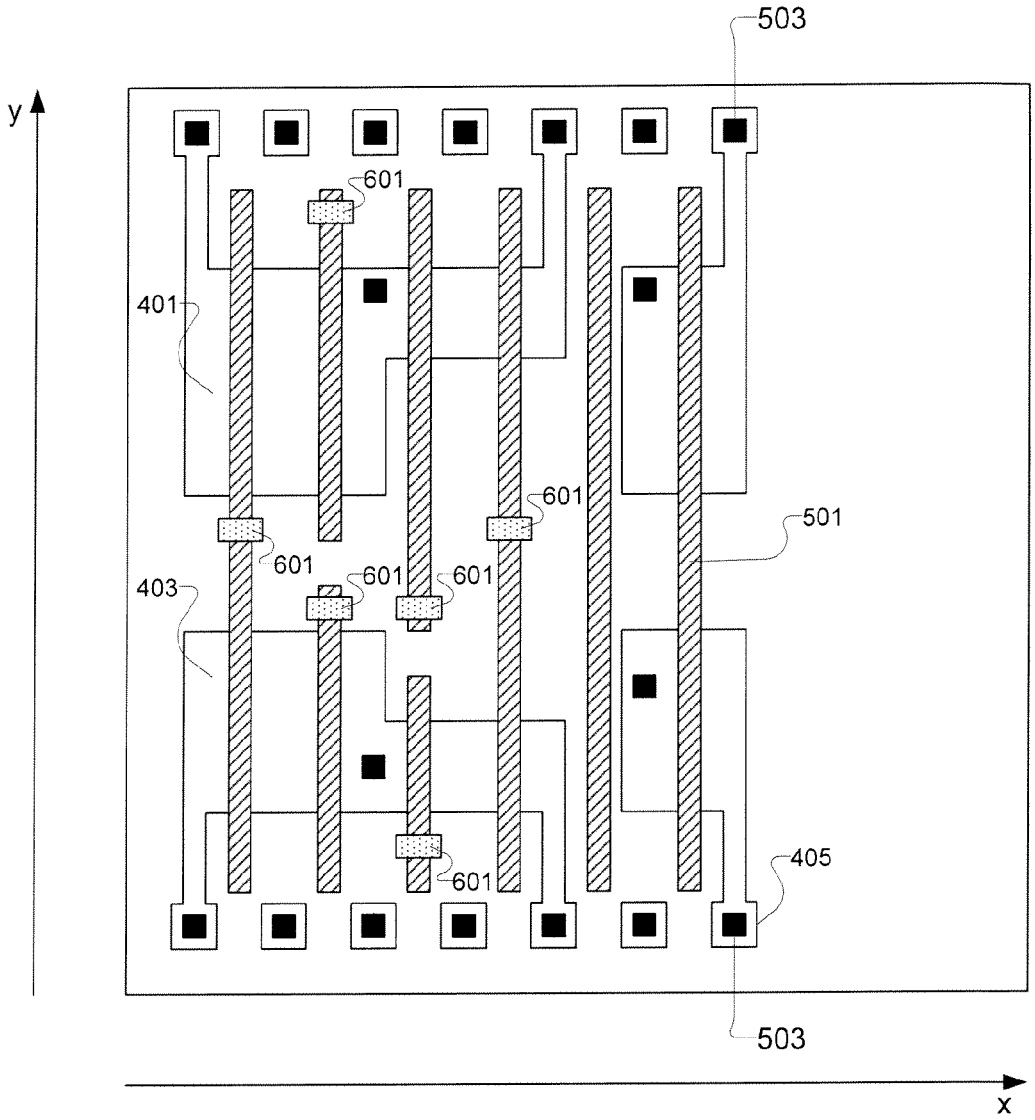



Fig. 6

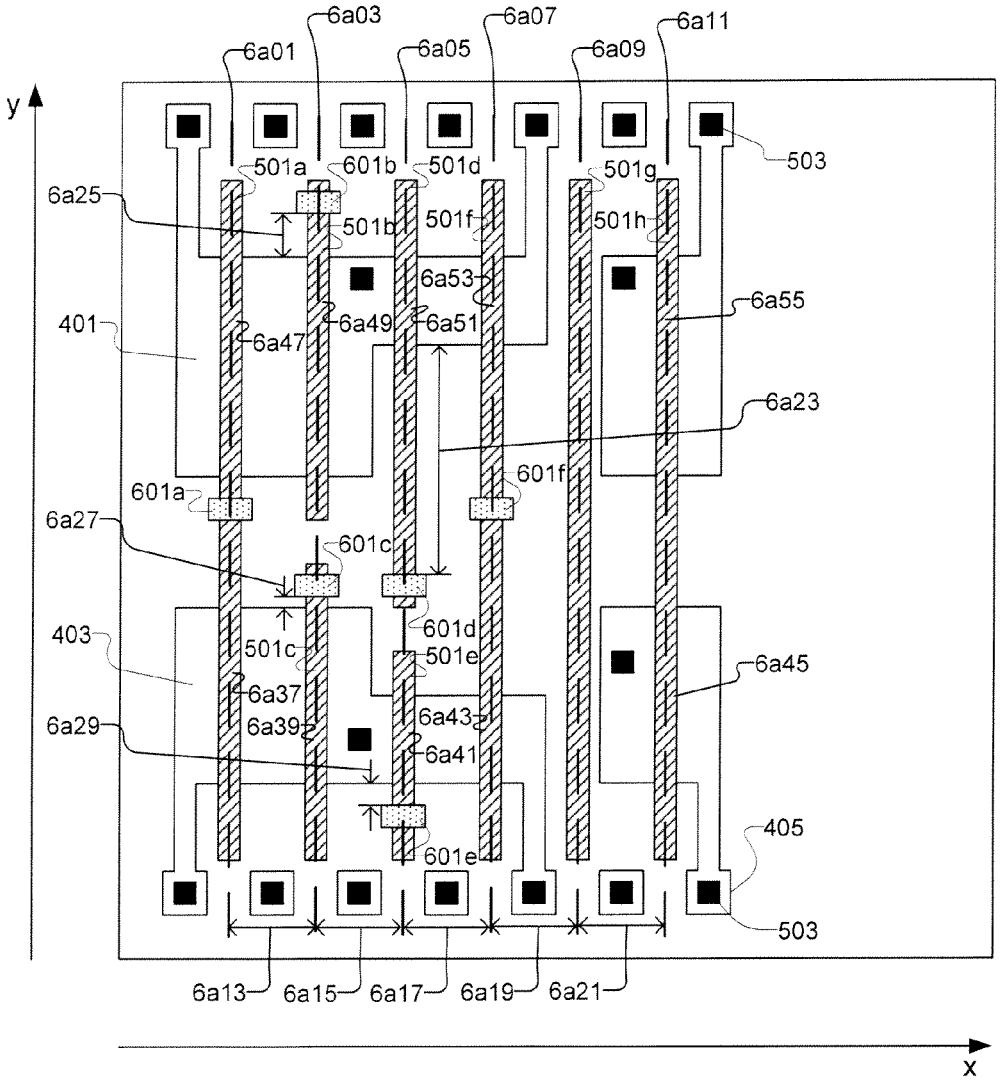

6a03
6a07
6a11
6a01
6a05
6a09
y
503
501a
601b
501d
501g
6a25
501b
501f
501h
6a53
6a55
401
6a49
6a51
6a47
6a23
601f
601a
6a27
601c
501c
601d
501e
403
6a45
6a37
6a43
6a39
6a29
6a41
405
601e
503
6a13
6a15
6a17
6a19
6a21
x

Fig. 6A

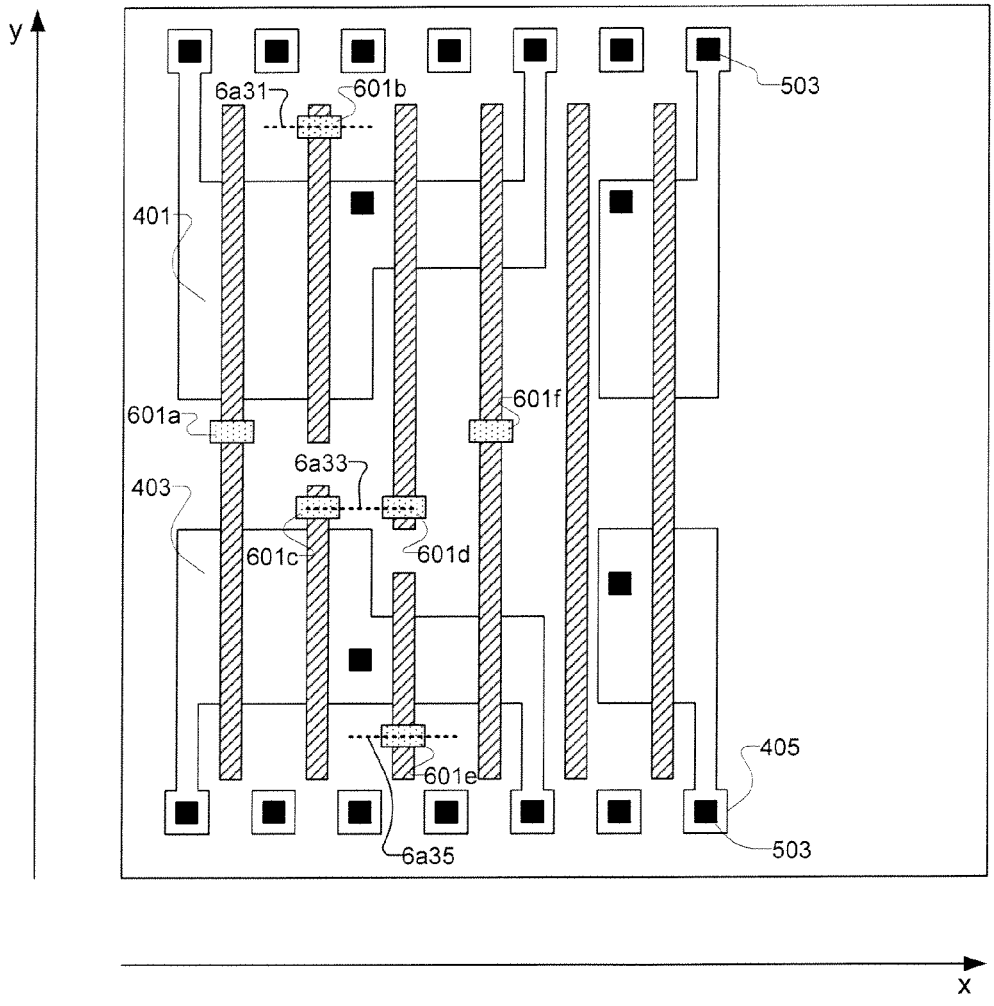

y
x
6a31
601b
503
401
601a
601f
6a33
403
601c
601d
405
601e
6a35
503

Fig. 6B

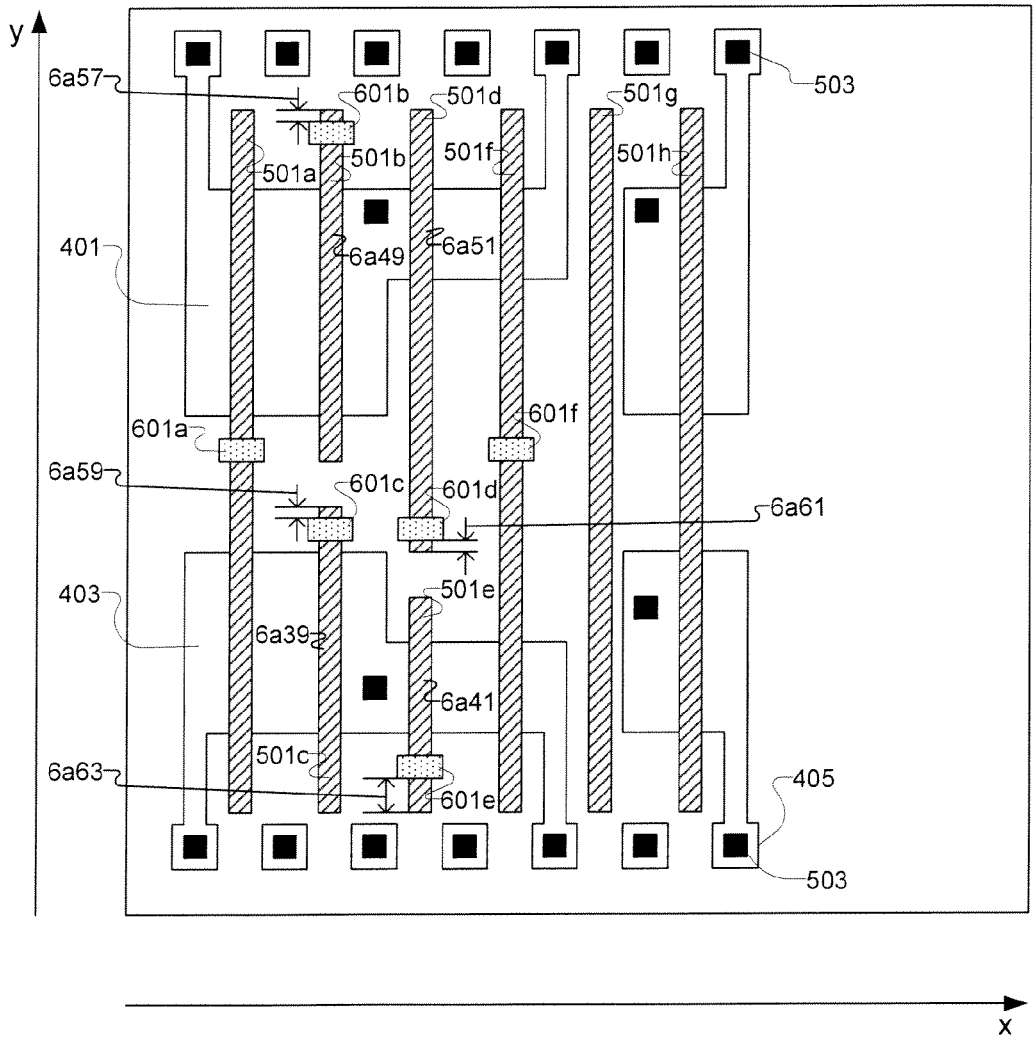

y
x
6a57
601b
501d
501g
503
501a
501b
501f
501h
401
6a49
6a51
601a
601f
6a59
601c
601d
6a61
403
501e
6a39
6a41
501c
6a63
601e
405
503

Fig. 6C

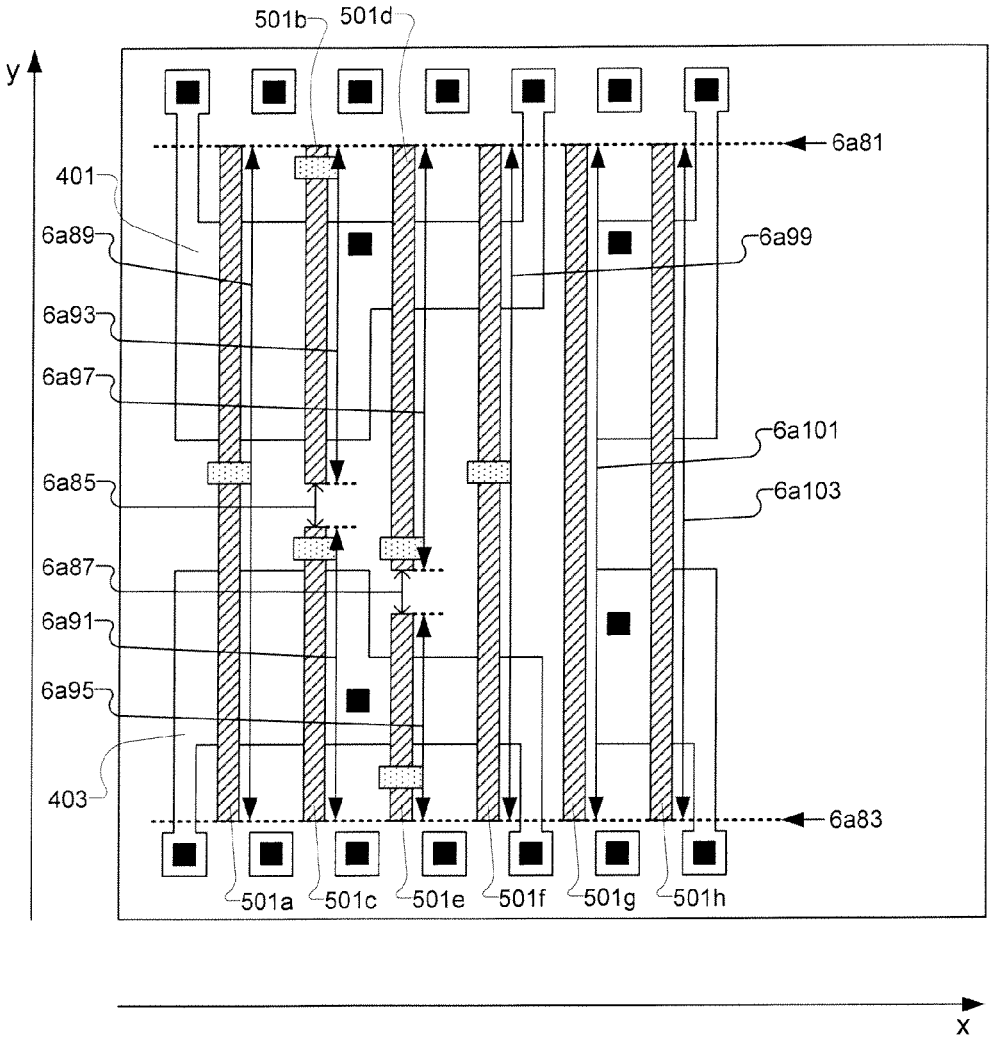

501b
501d
y
6a81
401
6a89
6a99
6a93
6a97
6a101
6a85
6a103
6a87
6a91
6a95
403
6a83
501a
501c
501e
501f
501g
501h
x

Fig. 6D

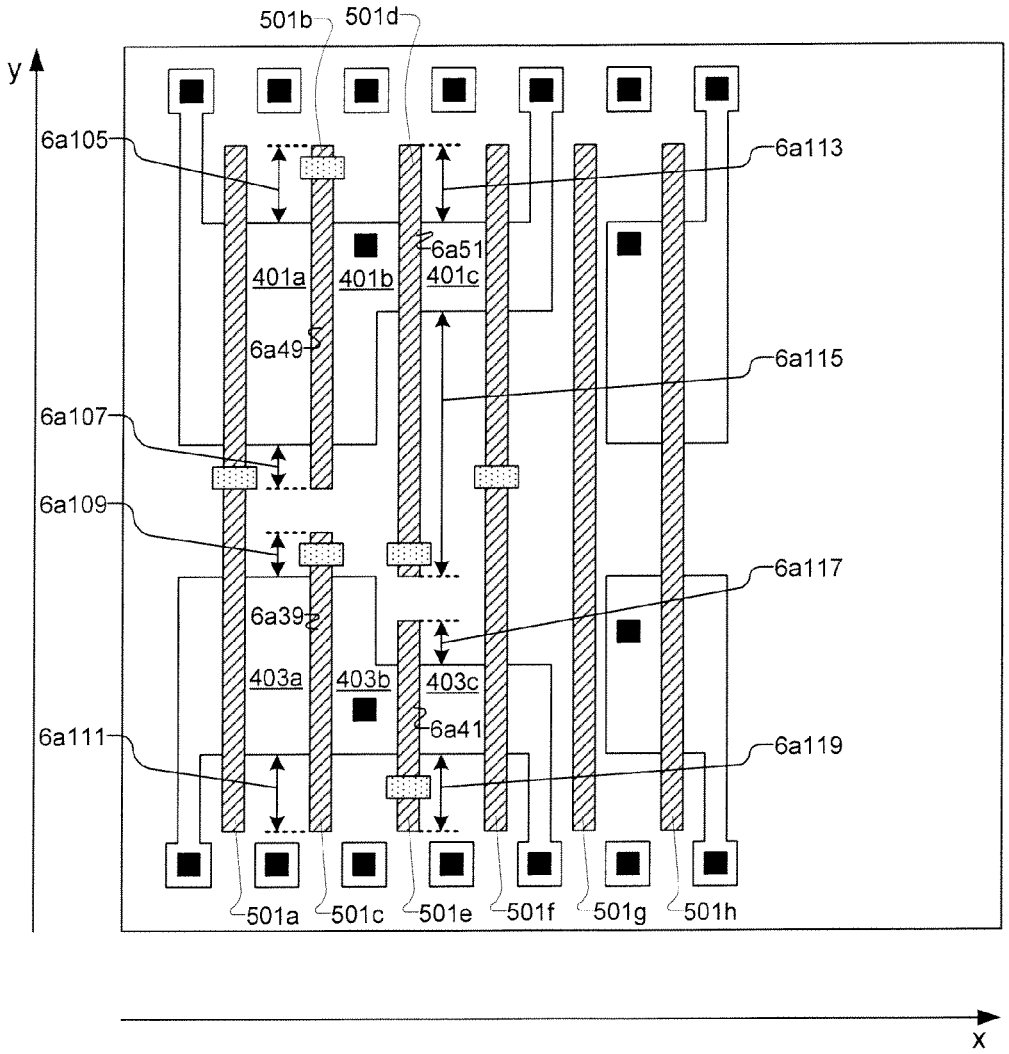

501b
501d
y
6a105
6a113
401a
401b
6a51
401c
6a49
6a115
6a107
6a109
6a117
6a39
403a
403b
403c
6a41
6a111
6a119
501a
501c
501e
501f
501g
501h
x

Fig. 6E

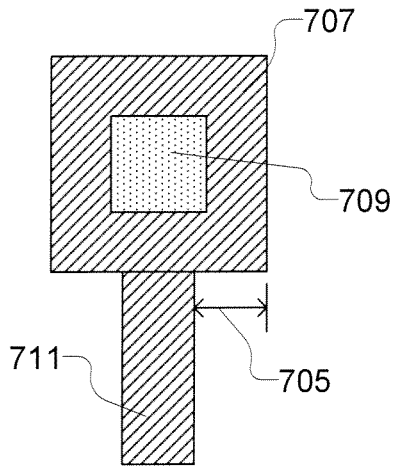



Fig. 7A

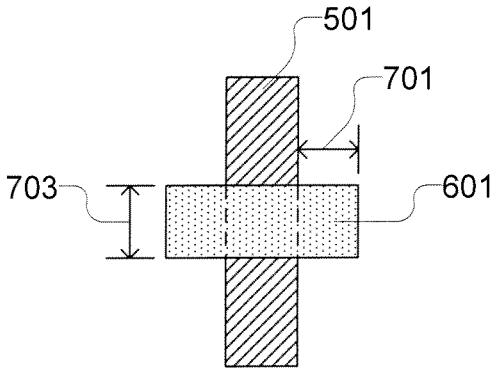



Fig. 7B

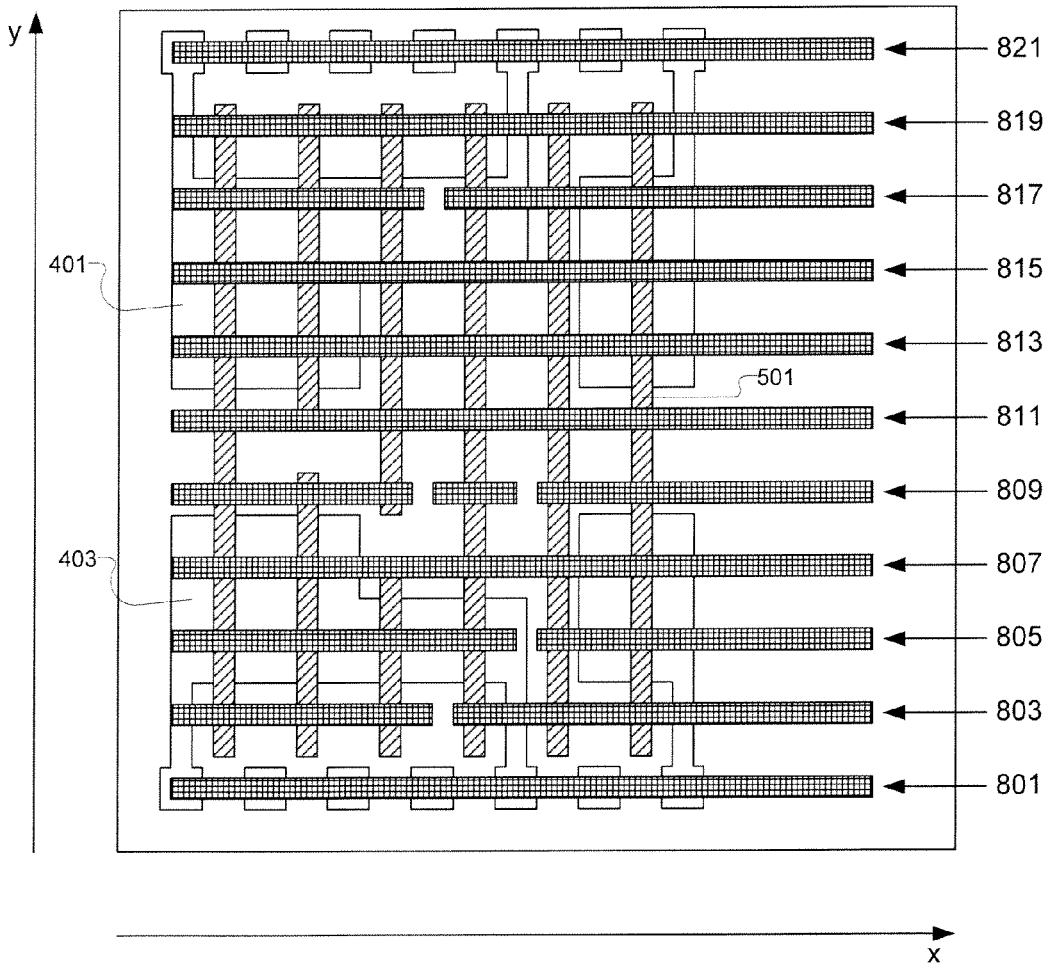



Fig. 8A

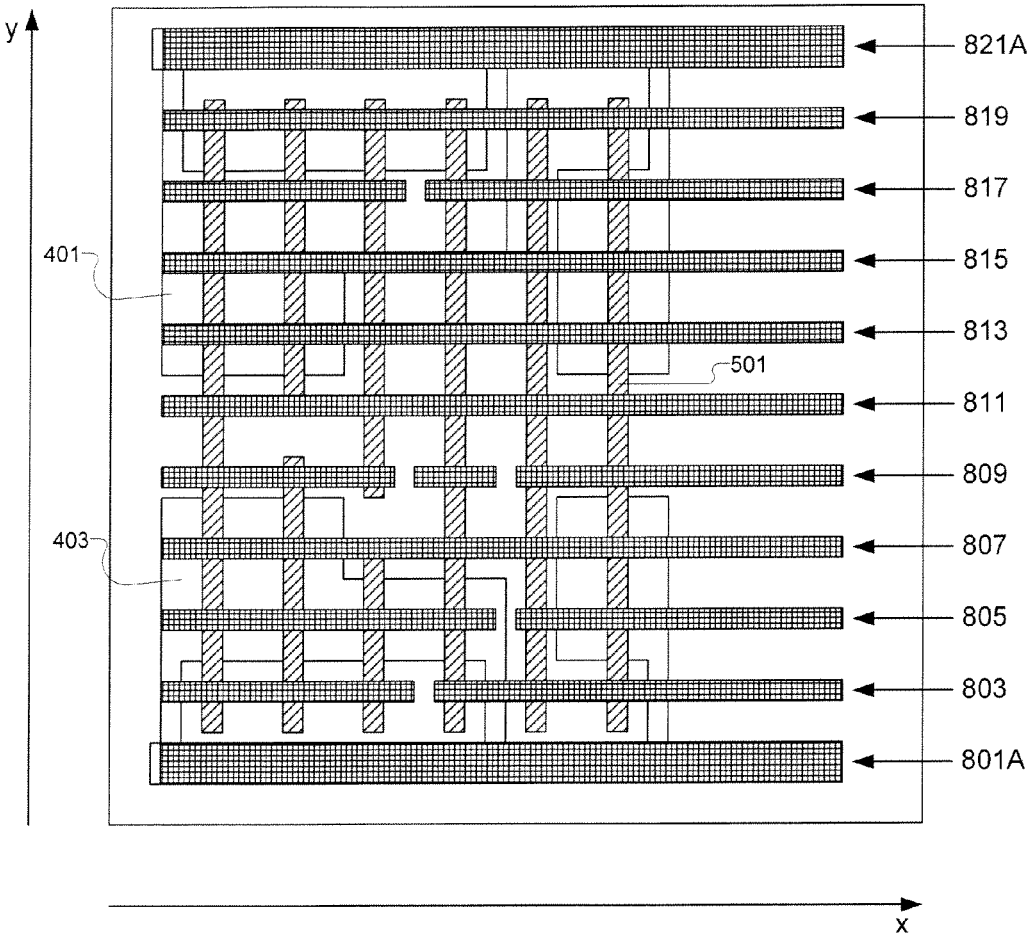



Fig. 8B

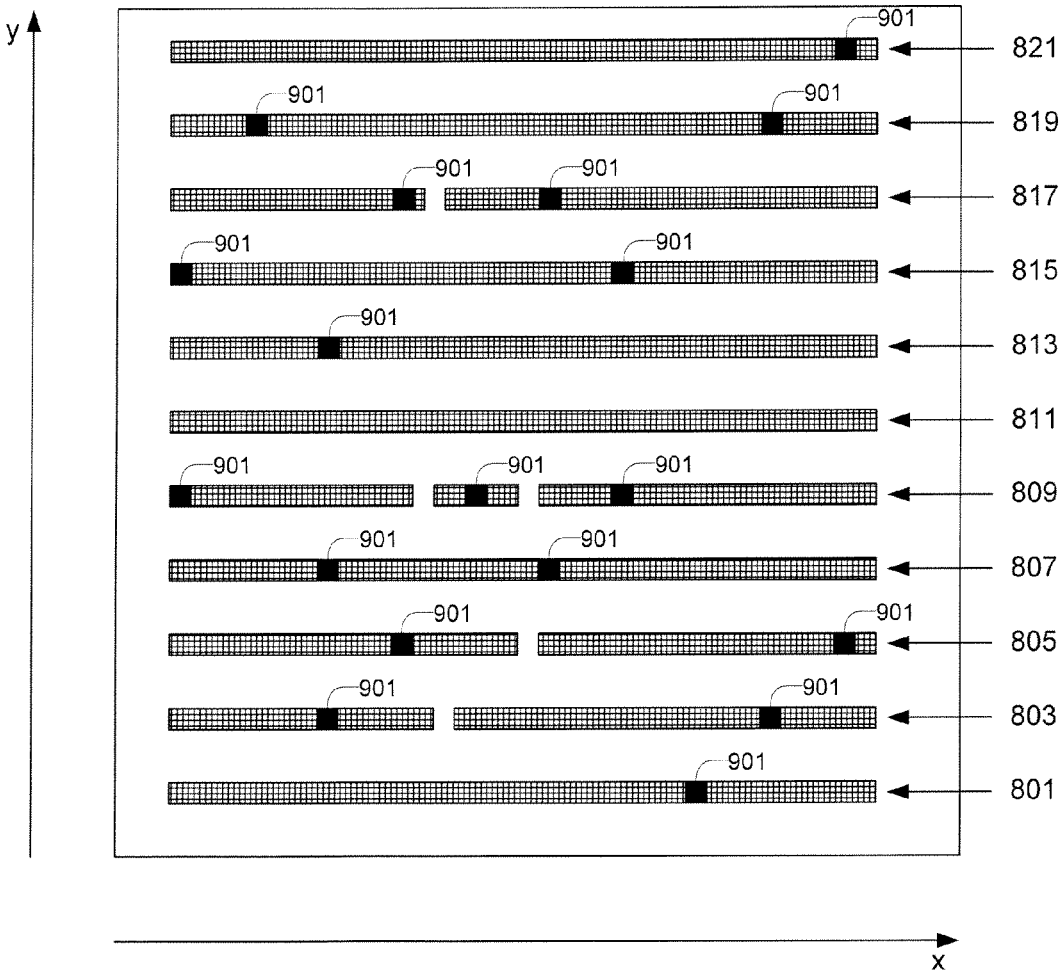



Fig. 9

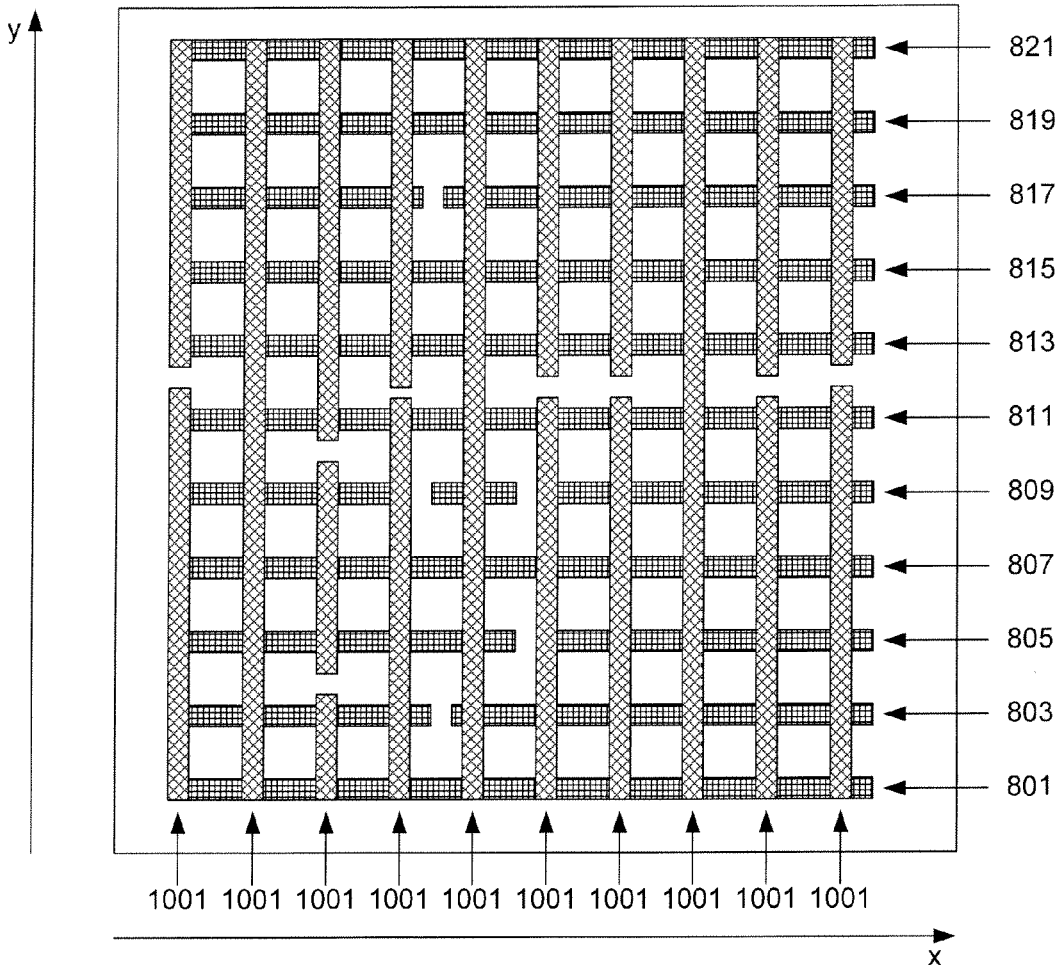

y
821
819
817
815
813
811
809
807
805
803
801
1001 1001 1001 1001 1001 1001 1001 1001 1001 1001
x

Fig. 10

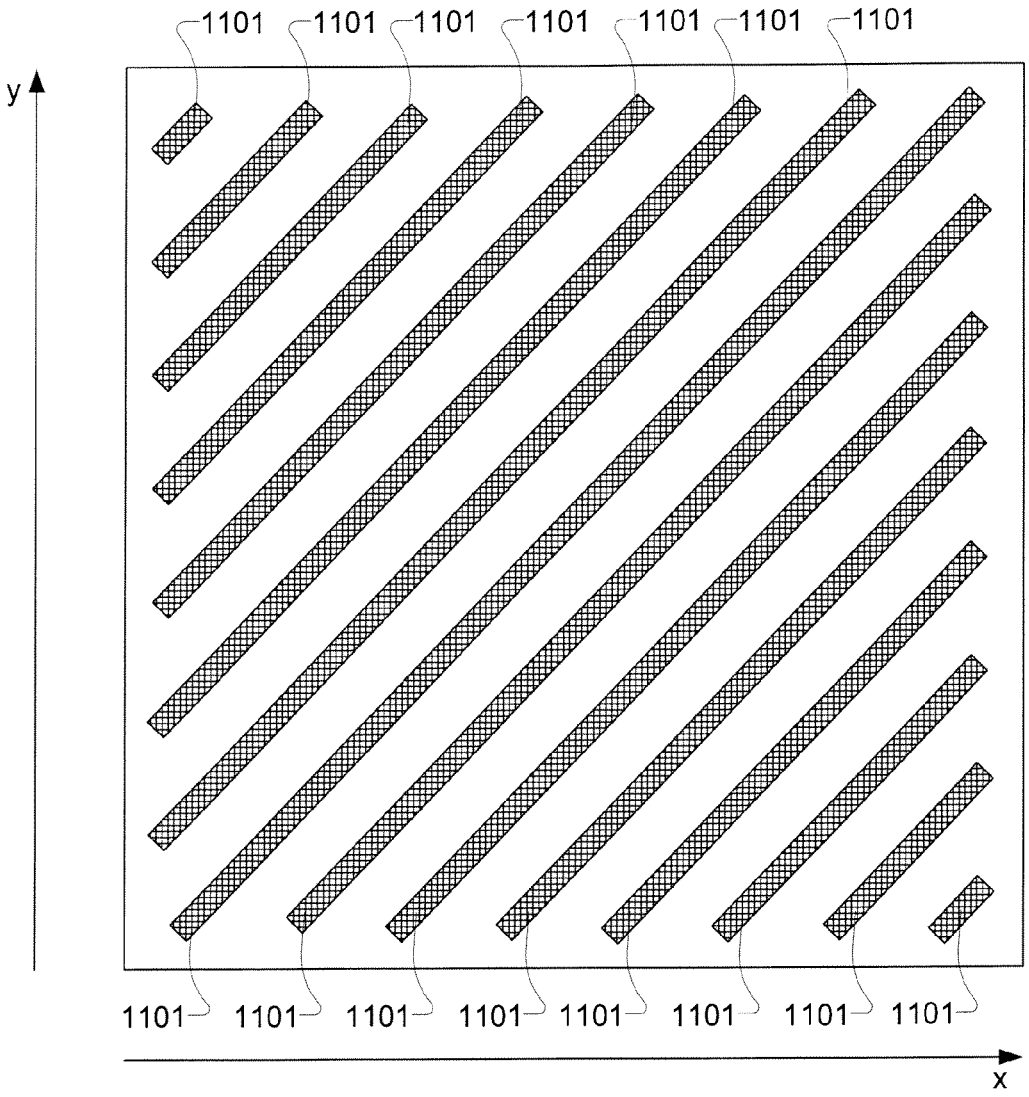

1101
1101
1101
1101
1101
1101
1101
y
1101
1101
1101
1101
1101
1101
1101
1101
x

Fig. 11

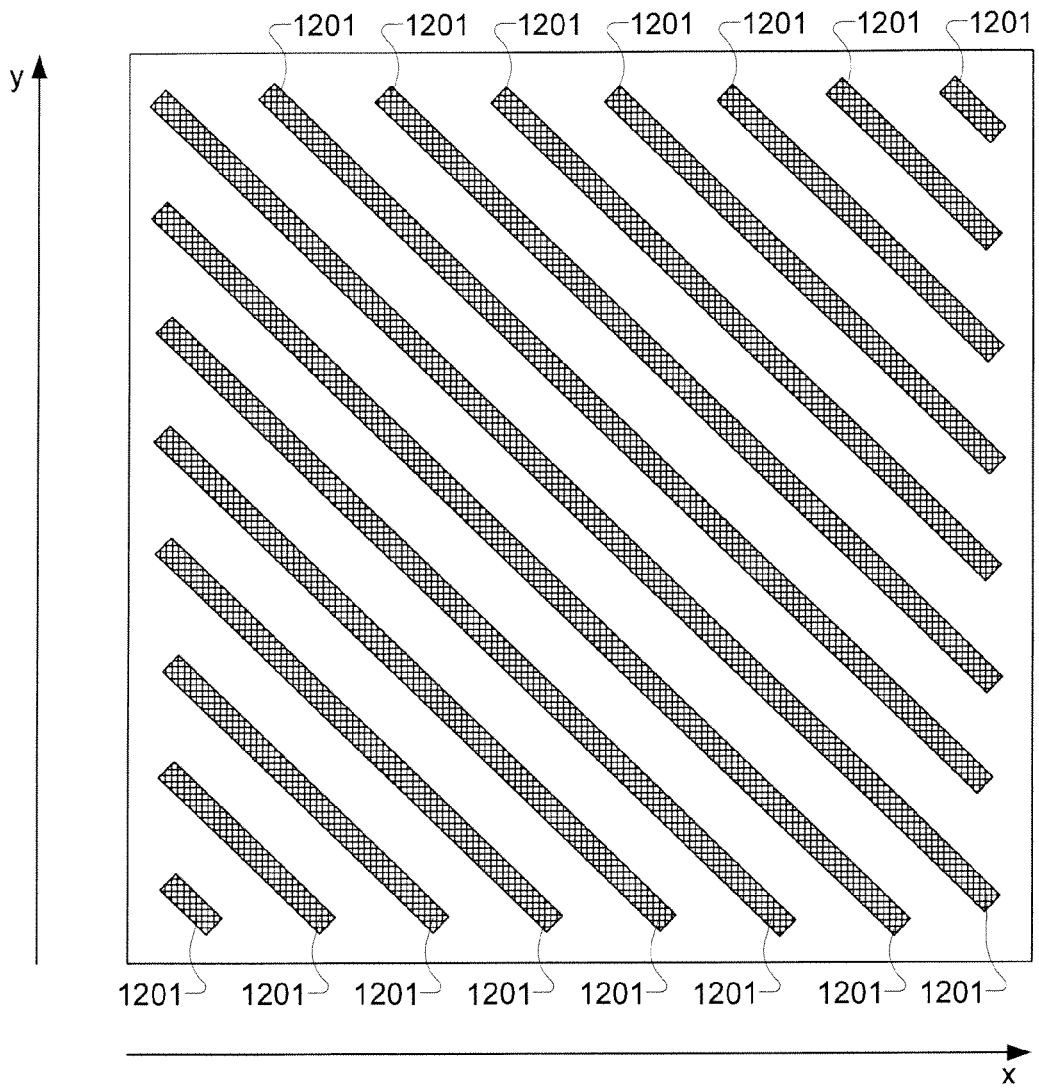

1201
1201
1201
1201
1201
1201
1201
y
1201
1201
1201
1201
1201
1201
1201
1201
x

Fig. 12

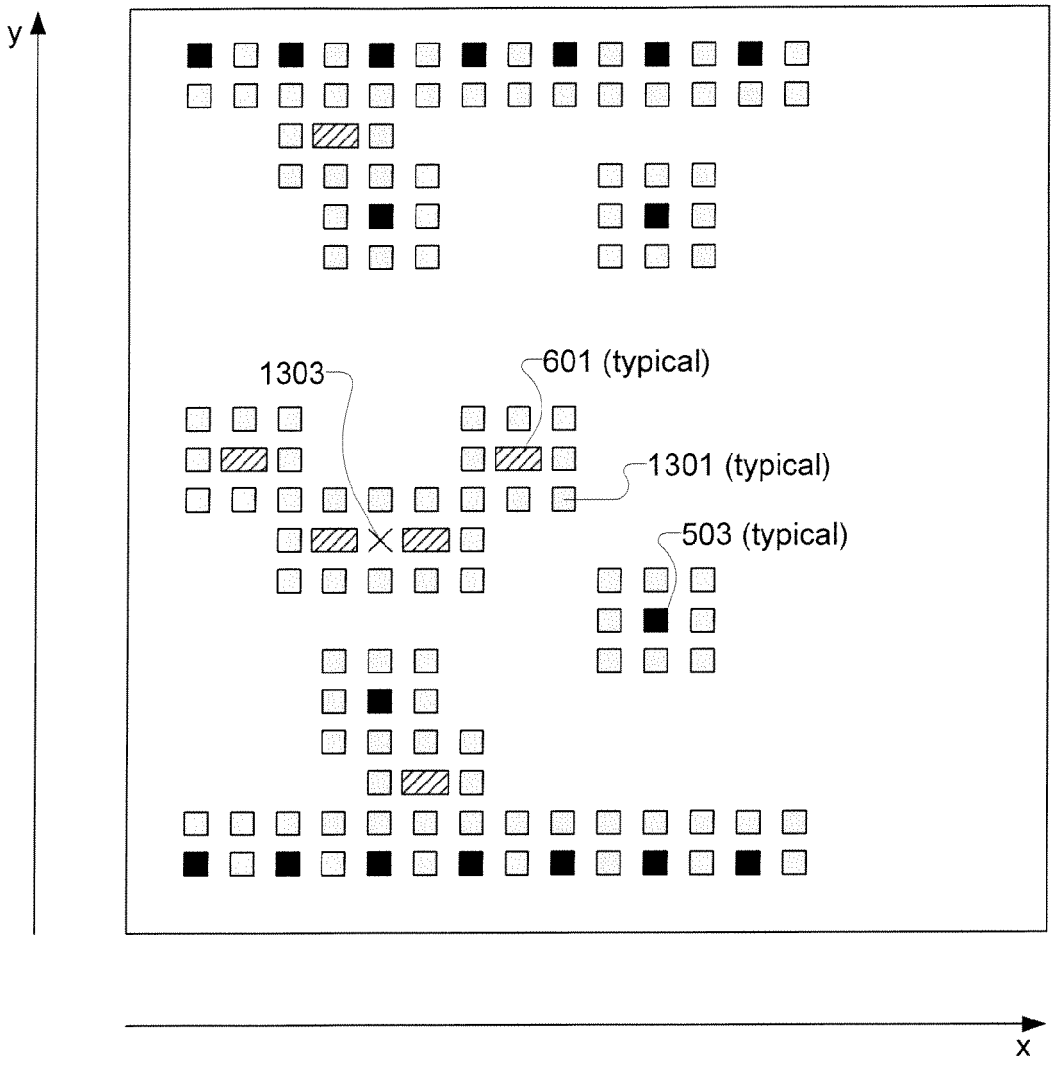



Fig. 13A

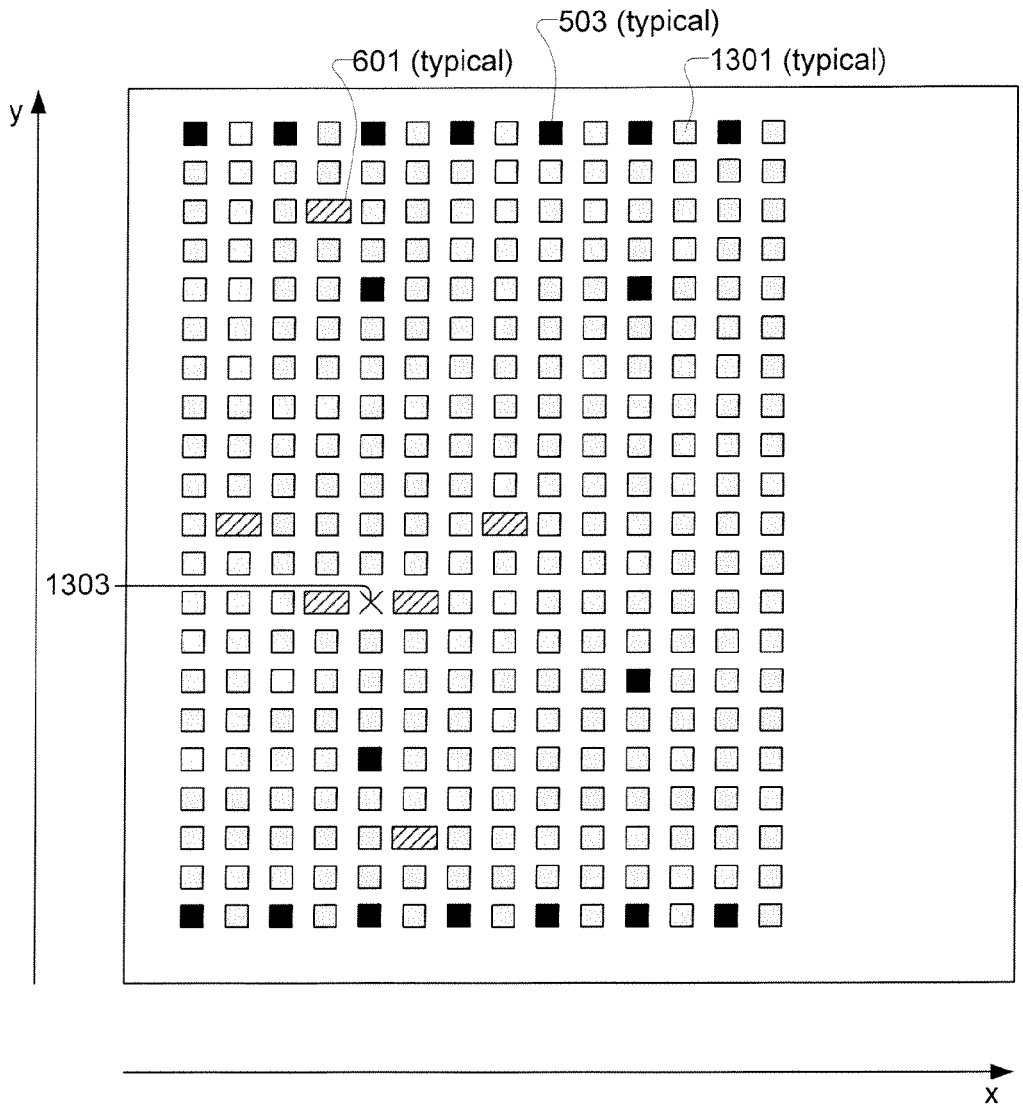



Fig. 13B

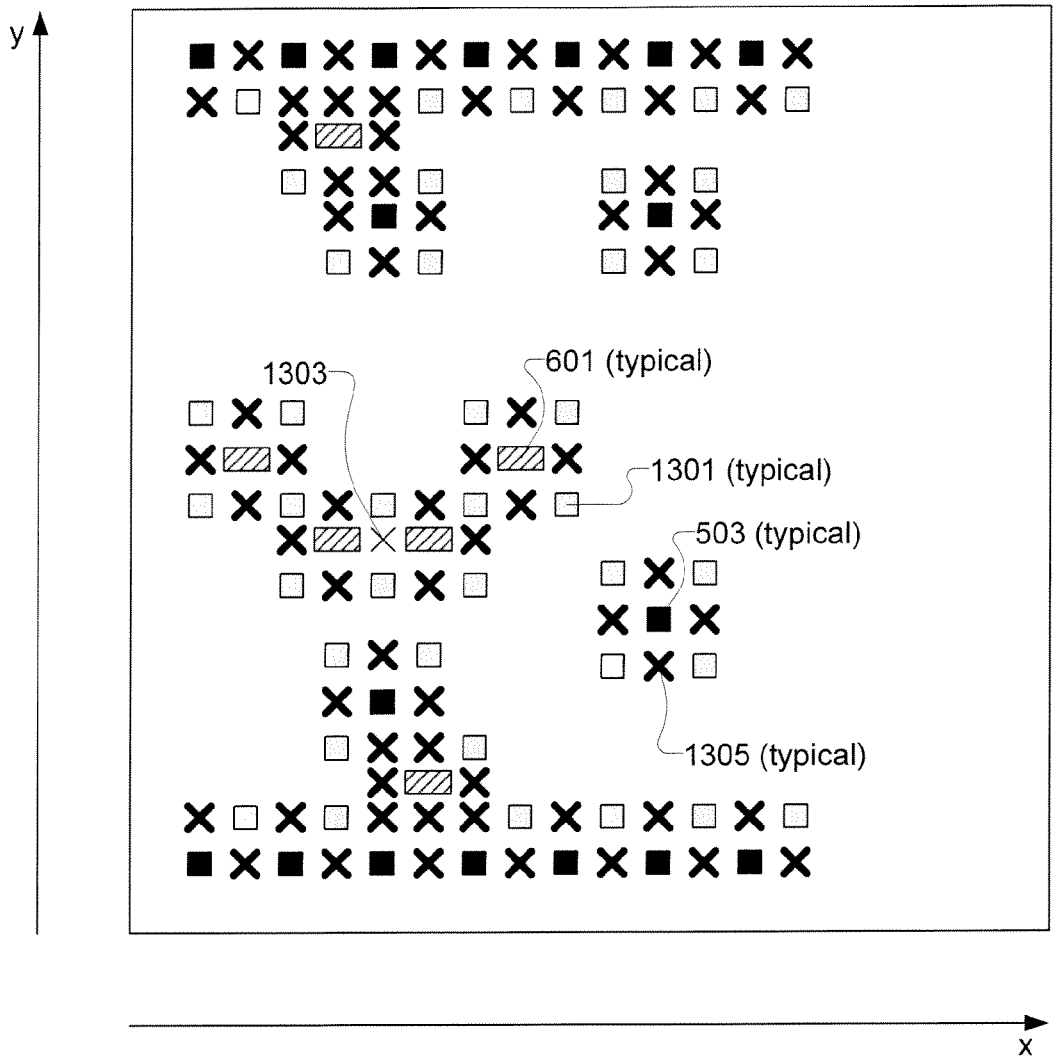



Fig. 13C

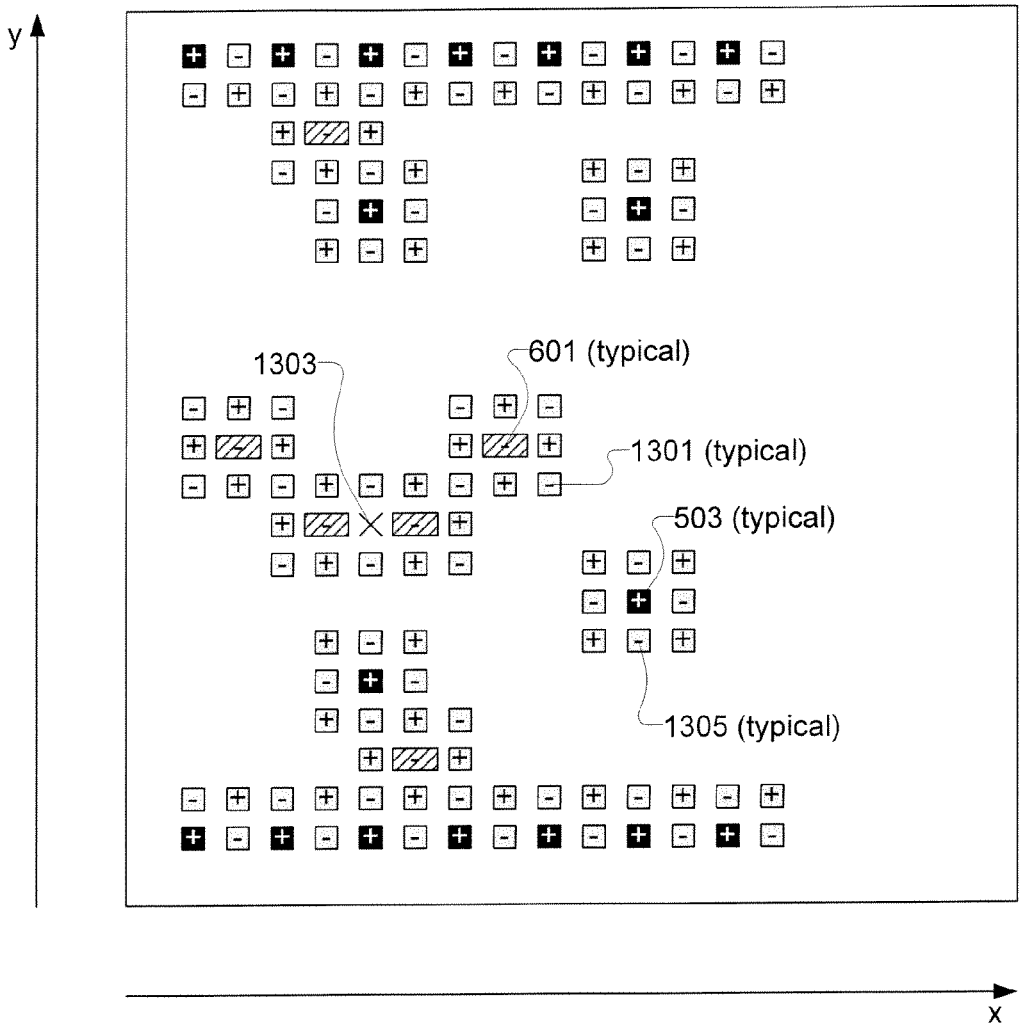



Fig. 13D

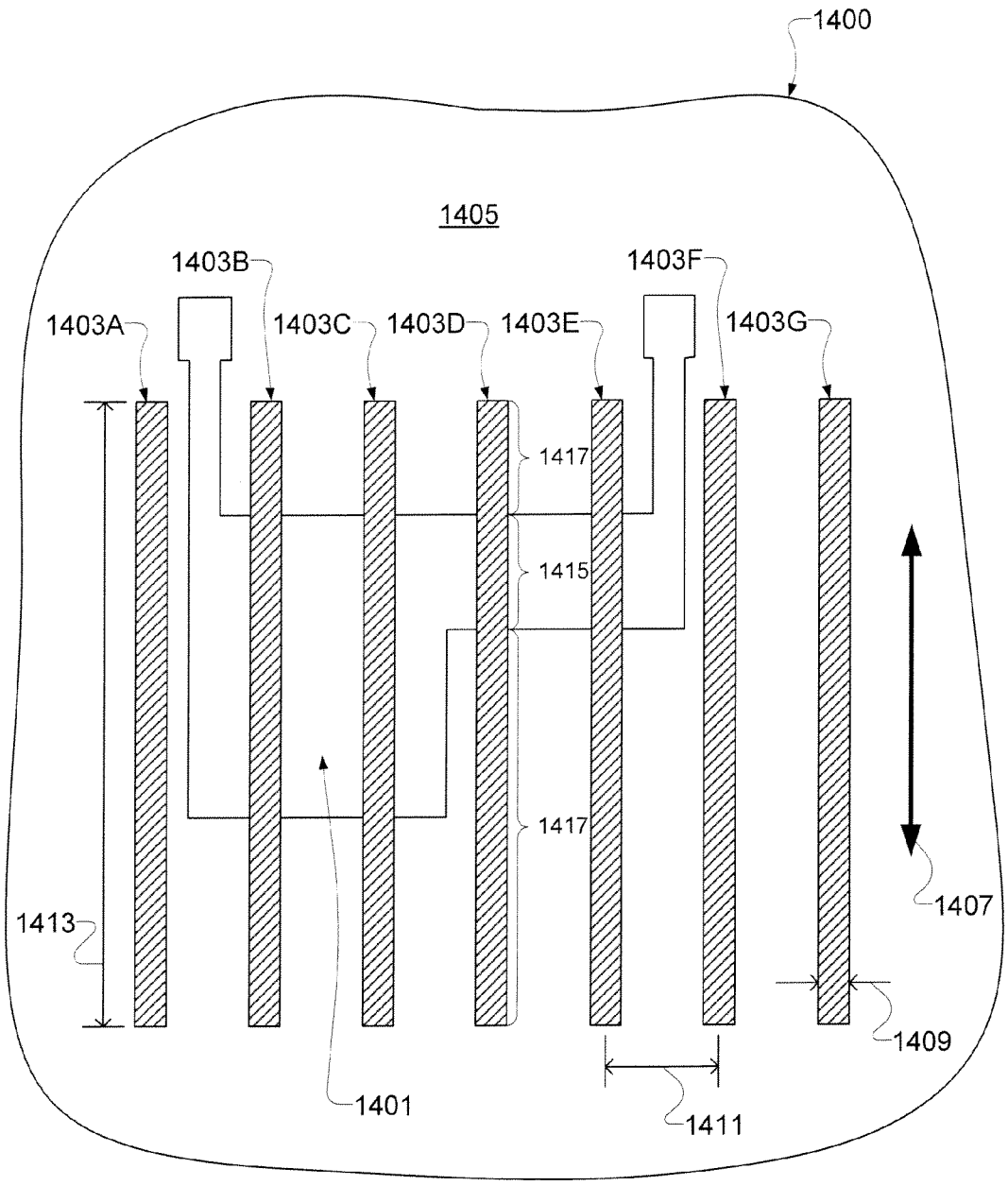

1400
1405
1403A
1403B
1403C
1403D
1403E
1403F
1403G
1417
1415
1417
1413
1407
1409
1401
1411

Fig. 14

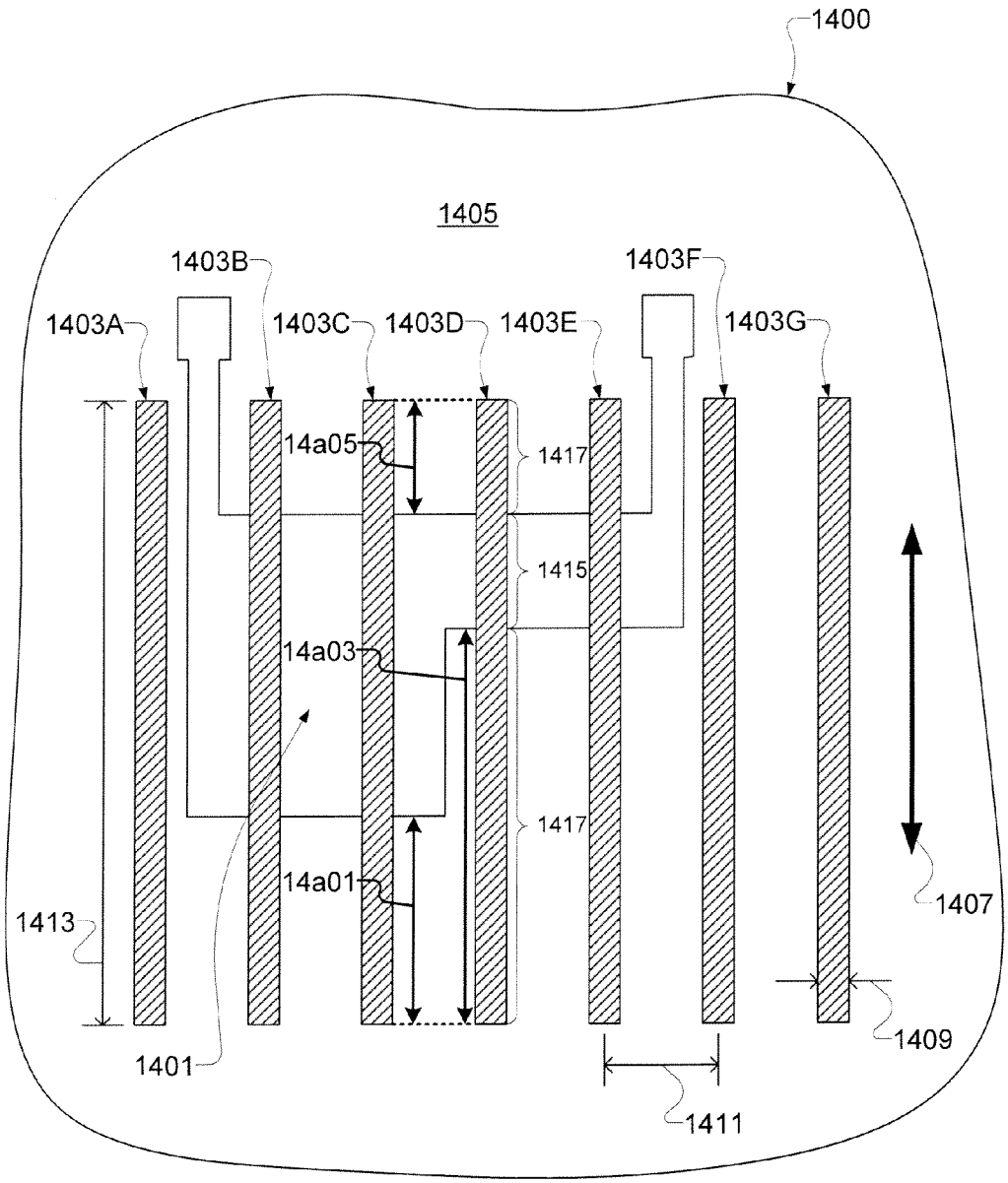
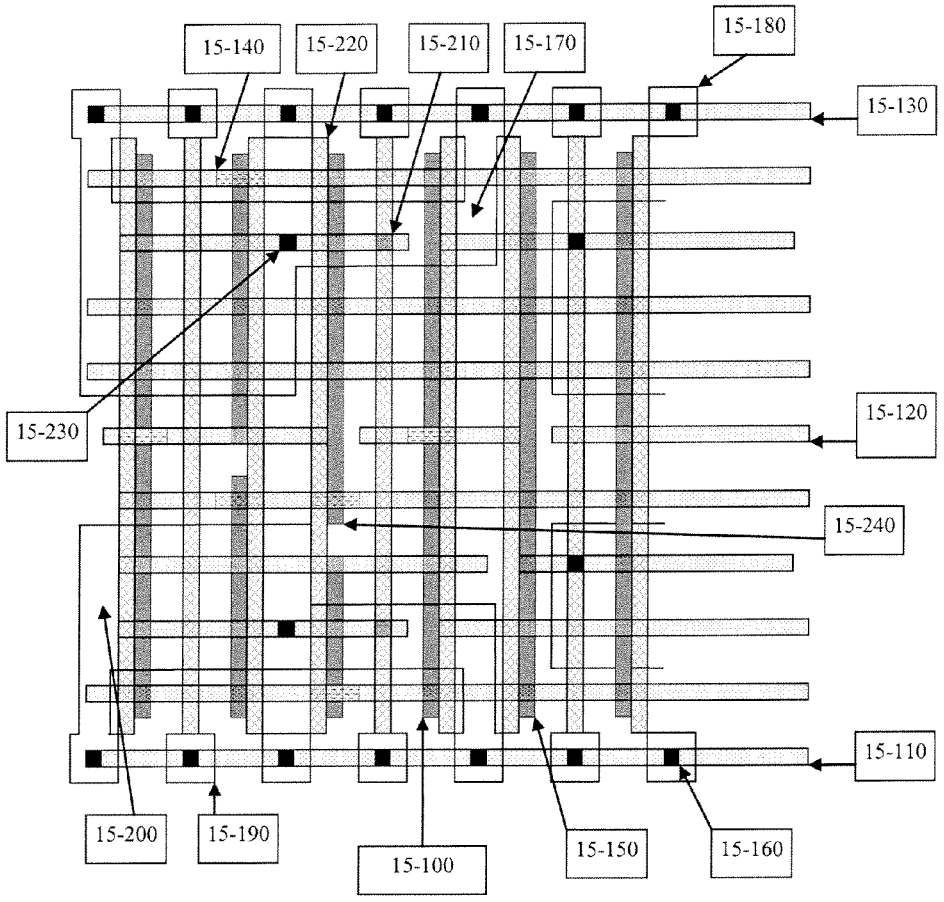

1400
1405
1403A
1403B
1403C
1403D
1403E
1403F
1403G
14a05
1417
1415
14a03
1417
14a01
1413
1401
1407
1409
1411

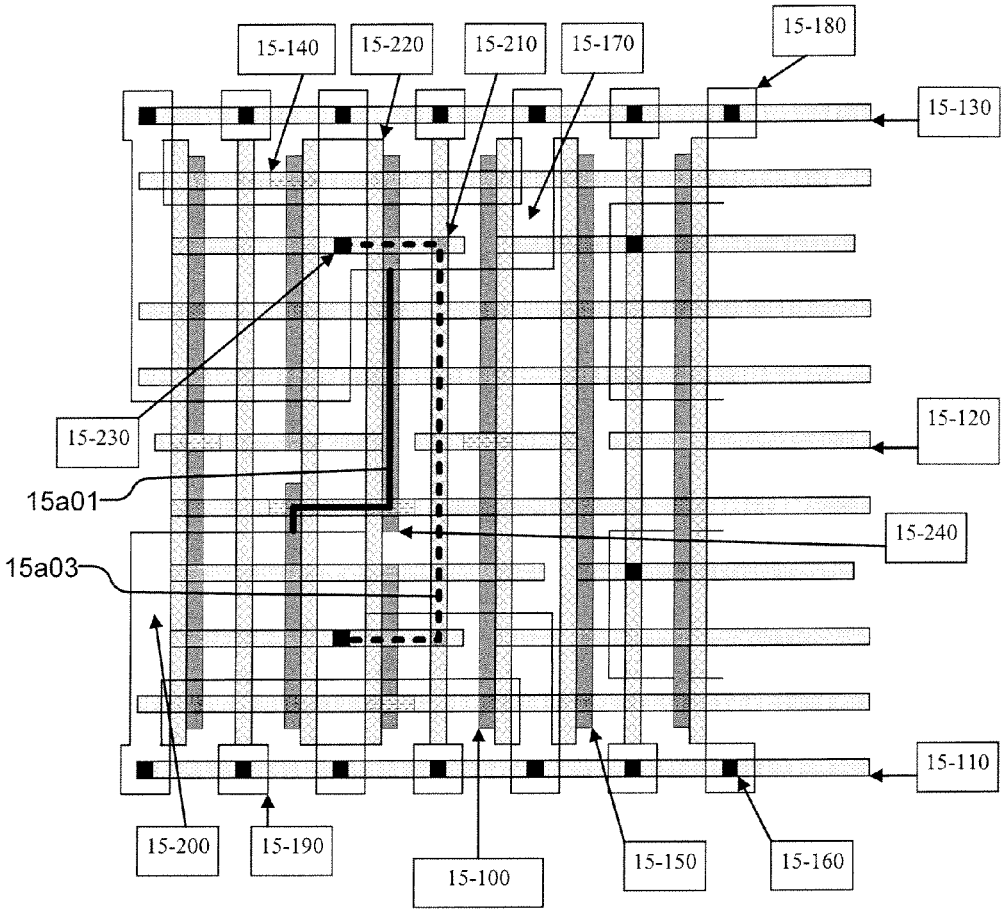
Fig. 14A




**Legend for the Individual Layers of Figure 15**

| Layer | Pattern |
|---|---|
| Diffusion (15-170, 15-180, 15-190, 15-200) | |
| Diffusion Contact (15-160, 15-230) | |
| Poly Silicon (15-100, 15-150) | |
| Poly Contact (15-140) | |
| Metal 1 (15-110, 15-120, 15-130) | |
| Via (15-210) | |
| Metal 2 (15-220) | |

Fig. 15




**Legend for the Individual Layers of Figure 15**

| Layer | Pattern |
|---|---|
| Diffusion (15-170, 15-180, 15-190, 15-200) | |
| Diffusion Contact (15-160, 15-230) | |
| Poly Silicon (15-100, 15-150) | |
| Poly Contact (15-140) | |
| Metal 1 (15-110, 15-120, 15-130) | |
| Via (15-210) | |
| Metal 2 (15-220) | |

Fig. 15A

# SEMICONDUCTOR CHIP INCLUDING INTEGRATED CIRCUIT INCLUDING FOUR TRANSISTORS OF FIRST TRANSISTOR TYPE AND FOUR TRANSISTORS OF SECOND TRANSISTOR TYPE WITH ELECTRICAL CONNECTIONS BETWEEN VARIOUS TRANSISTORS AND METHODS FOR MANUFACTURING THE SAME

## CLAIM OF PRIORITY

This application is a continuation application under 35 U.S.C. 120 of prior U.S. application Ser. No. 13/774,919, filed on Feb. 22, 2013, which is a continuation application under 35 U.S.C. 120 of prior U.S. application Ser. No. 12/572,225, filed on Oct. 1, 2009, issued as U.S. Pat. No. 8,436,400, on May 7, 2013, which is a continuation application under 35 U.S.C. 120 of prior U.S. application Ser. No. 12/212,562, filed Sep. 17, 2008, issued as U.S. Pat. No. 7,842,975, on Nov. 30, 2010, which is a continuation application under 35 U.S.C. 120 of prior U.S. application Ser. No. 11/683,402, filed Mar. 7, 2007, issued as U.S. Pat. No. 7,446,352, on Nov. 4, 2008, which claims priority under 35 U.S.C. 119(e) to U.S. Provisional Patent Application No. 60/781,288, filed Mar. 9, 2006. Each of the above-identified applications is incorporated herein by reference in its entirety.

## CROSS-REFERENCE TO RELATED APPLICATIONS

This application is related to each application identified in the table below. The disclosure of each application identified in the table below is incorporated herein by reference in its entirety.

| application Ser. No. | Filing Date |
|---|---|
| 12/561,207 | Sep. 16, 2009 |
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| 12/561,220 | Sep. 16, 2009 |
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| 12/561,234 | Sep. 16, 2009 |
| 12/561,238 | Sep. 16, 2009 |
| 12/561,243 | Sep. 16, 2009 |
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| 12/563,042 | Sep. 18, 2009 |
| 12/563,051 | Sep. 18, 2009 |
| 12/563,056 | Sep. 18, 2009 |
| 12/563,061 | Sep. 18, 2009 |
| 12/563,063 | Sep. 18, 2009 |
| 12/563,066 | Sep. 18, 2009 |
| 12/563,074 | Sep. 18, 2009 |
| 12/563,076 | Sep. 18, 2009 |
| 12/563,077 | Sep. 18, 2009 |
| 12/567,528 | Sep. 25, 2009 |
| 12/567,542 | Sep. 25, 2009 |
| 12/567,555 | Sep. 25, 2009 |
| 12/567,565 | Sep. 25, 2009 |
| 12/567,574 | Sep. 25, 2009 |
| 12/567,586 | Sep. 25, 2009 |
| 12/567,597 | Sep. 25, 2009 |
| 12/567,602 | Sep. 25, 2009 |
| 12/567,609 | Sep. 25, 2009 |
| 12/567,616 | Sep. 25, 2009 |
| 12/567,623 | Sep. 25, 2009 |
| 12/567,630 | Sep. 25, 2009 |
| 12/567,634 | Sep. 25, 2009 |
| 12/567,641 | Sep. 25, 2009 |
| 12/567,648 | Sep. 25, 2009 |



-continued

| application Ser. No. | Filing Date |
|---|---|
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| 12/571,343 | Sep. 30, 2009 |
| 12/571,351 | Sep. 30, 2009 |
| 12/571,357 | Sep. 30, 2009 |
| 12/571,998 | Oct. 1, 2009 |
| 12/572,011 | Oct. 1, 2009 |
| 12/572,022 | Oct. 1, 2009 |
| 12/572,046 | Oct. 1, 2009 |
| 12/572,055 | Oct. 1, 2009 |
| 12/572,061 | Oct. 1, 2009 |
| 12/572,068 | Oct. 1, 2009 |
| 12/572,077 | Oct. 1, 2009 |
| 12/572,091 | Oct. 1, 2009 |
| 12/572,194 | Oct. 1, 2009 |
| 12/572,201 | Oct. 1, 2009 |
| 12/572,212 | Oct. 1, 2009 |
| 12/572,218 | Oct. 1, 2009 |
| 12/572,221 | Oct. 1, 2009 |
| 12/572,225 | Oct. 1, 2009 |
| 12/572,228 | Oct. 1, 2009 |
| 12/572,229 | Oct. 1, 2009 |
| 12/572,232 | Oct. 1, 2009 |
| 12/572,237 | Oct. 1, 2009 |
| 12/572,239 | Oct. 1, 2009 |
| 12/572,243 | Oct. 1, 2009 |
| 13/774,919 | Feb. 22, 2013 |
| 13/774,940 | Feb. 22, 2013 |
| 13/774,954 | Feb. 22, 2013 |
| 13/774,970 | Feb. 22, 2013 |
| 13/827,615 | Mar. 14, 2013 |
| 13/827,755 | Mar. 14, 2013 |
| 13/834,302 | Mar. 15, 2013 |
| 13/837,123 | Mar. 15, 2013 |
| 14/304,778 | Jun. 13, 2014 |
| 14/711,731 | May 13, 2015 |
| 12/013,342 | Jan. 11, 2008 |
| 13/073,994 | Mar. 28, 2011 |
| 14/276,528 | May 13, 2014 |
| 12/013,356 | Jan. 11, 2008 |
| 13/047,474 | Mar. 14, 2011 |
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## BACKGROUND

A push for higher performance and smaller die size drives the semiconductor industry to reduce circuit chip area by approximately 50% every two years. The chip area reduction provides an economic benefit for migrating to newer technologies. The 50% chip area reduction is achieved by reducing the feature sizes between 25% and 30%. The reduction in feature size is enabled by improvements in manufacturing equipment and materials. For example, improvement in the lithographic process has enabled smaller feature sizes to be achieved, while improvement in chemical mechanical polishing (CMP) has in-part enabled a higher number of interconnect layers.

In the evolution of lithography, as the minimum feature size approached the wavelength of the light source used to expose the feature shapes, unintended interactions occurred between neighboring features. Today minimum feature sizes are approaching 45 nm (nanometers), while the wavelength of the light source used in the photolithography process remains at 193 nm. The difference between the minimum feature size and the wavelength of light used in the photolithography process is defined as the lithographic gap. As the lithographic gap grows, the resolution capability of the lithographic process decreases.

An interference pattern occurs as each shape on the mask interacts with the light. The interference patterns from neighboring shapes can create constructive or destructive interference. In the case of constructive interference, unwanted shapes may be inadvertently created. In the case of destructive interference, desired shapes may be inadvertently removed. In either case, a particular shape is printed in a different manner than intended, possibly causing a device failure. Correction methodologies, such as optical proximity correction (OPC), attempt to predict the impact from neighboring shapes and modify the mask such that the printed shape is fabricated as desired. The quality of the light interaction prediction is declining as process geometries shrink and as the light interactions become more complex.

In view of the foregoing, a solution is needed for managing lithographic gap issues as technology continues to progress toward smaller semiconductor device features sizes.

## SUMMARY

In one embodiment, an integrated circuit is disclosed to include a first gate electrode feature of a first gate electrode track. The first gate electrode feature of the first gate electrode track forms a first n-channel transistor as it crosses an n-diffusion region. The integrated circuit also includes a second gate electrode feature of the first gate electrode track. The second gate electrode feature of the first gate electrode track forms a first p-channel transistor as it crosses a p-diffusion region. The first and second gate electrode features of the first gate electrode track are separated by a first end-to-end spacing. The integrated circuit also includes a first gate electrode feature of a second gate electrode track. The first gate electrode feature of the second gate electrode track forms a second n-channel transistor as it crosses the n-diffusion region. The integrated circuit also includes a second gate electrode feature of the second gate electrode track. The second gate electrode feature of the second gate electrode track forms a second p-channel transistor as it crosses the p-diffusion region. The first and second gate electrode features of the second gate electrode track are separated by a second end-to-end spacing that is offset from the first end-to-end spacing such that a line of sight perpendicular to the first and second gate electrode tracks does not exist through the first and second end-to-end spacings.

In another embodiment, a cell of a semiconductor device is disclosed. The cell includes a substrate portion formed to include a plurality of diffusion regions. The plurality of diffusion regions respectively correspond to active areas of the substrate portion within which one or more processes are applied to modify one or more electrical characteristics of the active areas of the substrate portion. The plurality of diffusion regions are separated from each other by one or more non-active regions of the substrate portion.

Also in this embodiment, the cell includes a gate electrode level of the cell formed above the substrate portion. The gate electrode level includes a number of conductive features defined to extend in only a first parallel direction. Adjacent ones of the number of conductive features that share a common line of extent in the first parallel direction are fabricated from respective originating layout features that are separated from each other by an end-to-end spacing having a size measured in the first parallel direction. The size of each end-to-end spacing between originating layout features corresponding to adjacent ones of the number of conductive features within the gate electrode level of the cell is substantially equal and is minimized to an extent allowed by a semiconductor device manufacturing capability. The number of conductive features within the gate electrode level of the cell includes conductive features defined along at least four different virtual lines of extent in the first parallel direction across the gate electrode level of the cell.

A width size of the conductive features within the gate electrode level is measured perpendicular to the first parallel direction. The width size of the conductive features within a photolithographic interaction radius within the gate electrode level is less than a wavelength of light used in a photolithog-

raphy process to fabricate the conductive features within the gate electrode level. The wavelength of light used in the photolithography process is less than or equal to 193 nanometers. The photolithographic interaction radius is five wavelengths of light used in the photolithography process.

Some of the number of conductive features within the gate electrode level of the cell are defined to include one or more gate electrode portions which extend over one or more of the active areas of the substrate portion corresponding to the plurality of diffusion regions. Each gate electrode portion and a corresponding active area of the substrate portion over which it extends together define a respective transistor device.

Also in this embodiment, the cell includes a number of interconnect levels formed above the gate electrode level of the cell. The substrate portion, the gate electrode level of the cell, and the number of interconnect levels are spatially aligned such that structures fabricated within each of the substrate portion, the gate electrode level of the cell, and the number of interconnect levels spatially relate to connect as required to form functional electronic devices within the semiconductor device.

In one embodiment, a semiconductor chip includes a region including a plurality of transistors, where each of the plurality of transistors in the region forms part of circuitry associated with execution of one or more logic functions. The region includes at least ten conductive structures formed within the semiconductor chip, where some of the at least ten conductive structures form at least one transistor gate electrode. Each of the at least ten conductive structures respectively has a corresponding top surface, wherein an entirety of a periphery of the corresponding top surface is defined by a corresponding first end, a corresponding second end, a corresponding first edge, and a corresponding second edge, such that a total distance along the entirety of the periphery of the corresponding top surface is equal to a sum of a total distance along the corresponding first edge and a total distance along the corresponding second edge and a total distance along the corresponding first end and a total distance along the corresponding second end. The total distance along the corresponding first edge is greater than two times the total distance along the corresponding first end. The total distance along the corresponding first edge is greater than two times the total distance along the corresponding second end. The total distance along the corresponding second edge is greater than two times the total distance along the corresponding first end. The total distance along the corresponding second edge is greater than two times the total distance along the corresponding second end. The corresponding first end extends from the corresponding first edge to the corresponding second edge and is located principally within a space between the corresponding first and second edges. The corresponding second end extends from the corresponding first edge to the corresponding second edge and is located principally within the space between the corresponding first and second edges. The top surfaces of the at least ten conductive structures are co-planar with each other. Each of the at least ten conductive structures has a corresponding lengthwise centerline oriented in a first direction along its top surface and extending from its first end to its second end. Each of the at least ten conductive structures has a length as measured along its lengthwise centerline from its first end to its second end. The first edge of each of the at least ten conductive structures is substantially straight. The second edge of each of the at least ten conductive structures is substantially straight. Each of the at least ten conductive structures has both its first edge and its second edge oriented substantially parallel to its lengthwise centerline. Each of the at least ten conductive structures has a width measured in a second direction perpendicular to the first direction at a midpoint of its lengthwise centerline. Each of the first direction and the second direction is oriented substantially parallel to the co-planar top surfaces of the at least ten conductive structures. The at least ten conductive structures are positioned in a side-by-side manner such that each of the at least ten conductive structures is positioned to have at least a portion of its length beside at least a portion of the length of another of the at least ten conductive structures. The width of each of the at least ten conductive structures is less than 45 nanometers. The region has a size of about 965 nanometers as measured in the second direction. Each of the at least ten conductive structures is positioned such that a distance as measured in the second direction between its lengthwise centerline and the lengthwise centerline of at least one other of the at least ten conductive structures is substantially equal to a first pitch that is less than or equal to about 193 nanometers. The at least ten conductive structures includes a first conductive structure. The first conductive structure includes a portion that forms a gate electrode of first transistor of a first transistor type. The first conductive structure also includes a portion that forms a gate electrode of a first transistor of a second transistor type. The at least ten conductive structures includes a second conductive structure. The second conductive structure includes a portion that forms a gate electrode of a second transistor of the first transistor type, wherein any transistor having its gate electrode formed by the second conductive structure is of the first transistor type. The at least ten conductive structures includes a third conductive structure. The third conductive structure includes a portion that forms a gate electrode of a second transistor of the second transistor type, wherein any transistor having its gate electrode formed by the third conductive structure is of the second transistor type. The at least ten conductive structures includes a fourth conductive structure. The fourth conductive structure includes a portion that forms a gate electrode of a third transistor of the first transistor type, wherein any transistor having its gate electrode formed by the fourth conductive structure is of the first transistor type. The at least ten conductive structures includes a fifth conductive structure. The fifth conductive structure includes a portion that forms a gate electrode of a third transistor of the second transistor type, wherein any transistor having its gate electrode formed by the fifth conductive structure is of the second transistor type. The first transistor of the first transistor type includes a first diffusion terminal. The second transistor of the first transistor type includes a first diffusion terminal. The first diffusion terminal of the first transistor of the first transistor type is electrically connected to the first diffusion terminal of the second transistor of the first transistor type through a first electrical connection. The first transistor of the second transistor type includes a first diffusion terminal. The second transistor of the second transistor type includes a first diffusion terminal. The first diffusion terminal of the first transistor of the second transistor type is electrically connected to the first diffusion terminal of the second transistor of the second transistor type through a second electrical connection. The second transistor of the first transistor type includes a second diffusion terminal. The third transistor of the first transistor type includes a first diffusion terminal. The second diffusion terminal of the second transistor of the first transistor type is electrically connected to the first diffusion terminal of the third transistor of the first transistor type through a third electrical connection. The second transistor of the second transistor type includes a second diffusion terminal. The third transistor of the second transistor type includes a first diffusion terminal. The second diffusion terminal of the second transistor of the

second transistor type is electrically connected to the first diffusion terminal of the third transistor of the second transistor type through a fourth electrical connection. The third transistor of the first transistor type includes a second diffusion terminal electrically connected to a first diffusion terminal of a fourth transistor of the first transistor type through a fifth electrical connection. The third transistor of the second transistor type includes a second diffusion terminal electrically connected to a first diffusion terminal of a fourth transistor of the second transistor type through a sixth electrical connection. The third electrical connection is electrically connected to the fourth electrical connection through a seventh electrical connection. The gate electrode of the second transistor of the first transistor type is electrically connected to the gate electrode of the third transistor of the second transistor type through an eighth electrical connection. The gate electrode of the third transistor of the first transistor type is electrically connected to the gate electrode of the second transistor of the second transistor type through a ninth electrical connection. Each transistor of the first transistor type having its gate electrode formed by any of the at least ten conductive structures is included in a first collection of transistors. Each transistor of the second transistor type having its gate electrode formed by any of the at least ten conductive structures is included in a second collection of transistors. The first collection of transistors is separated from the second collection of transistors by an inner sub-region of the region. The inner sub-region does not include a source or a drain of any transistor.

Other aspects and advantages of the invention will become more apparent from the following detailed description, taken in conjunction with the accompanying drawings, illustrating by way of example the present invention.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is an illustration showing a number of neighboring layout features and a representation of light intensity used to render each of the layout features, in accordance with one embodiment of the present invention;

FIG. **2** is an illustration showing a generalized stack of layers used to define a dynamic array architecture, in accordance with one embodiment of the present invention;

FIG. **3**A is an illustration showing an exemplary base grid to be projected onto the dynamic array to facilitate definition of the restricted topology, in accordance with one embodiment of the present invention;

FIG. **3**B is an illustration showing separate base grids projected across separate regions of the die, in accordance with an exemplary embodiment of the present invention;

FIG. **3**C is an illustration showing an exemplary linear-shaped feature defined to be compatible with the dynamic array, in accordance with one embodiment of the present invention;

FIG. **3**D is an illustration showing another exemplary linear-shaped feature defined to be compatible with the dynamic array, in accordance with one embodiment of the present invention;

FIG. **4** is an illustration showing a diffusion layer layout of an exemplary dynamic array, in accordance with one embodiment of the present invention;

FIG. **5** is an illustration showing a gate electrode layer and a diffusion contact layer above and adjacent to the diffusion layer of FIG. **4**, in accordance with one embodiment of the present invention;

FIG. **6** is an illustration showing a gate electrode contact layer defined above and adjacent to the gate electrode layer of FIG. **5**, in accordance with one embodiment of the present invention;

FIGS. **6**A-**6**E show annotated versions of FIG. **6**;

FIG. **7**A is an illustration showing a traditional approach for making contact to the gate electrode;

FIG. **7**B is an illustration showing a gate electrode contact defined in accordance with one embodiment of the present invention;

FIG. **8**A is an illustration showing a metal **1** layer defined above and adjacent to the gate electrode contact layer of FIG. **6**, in accordance with one embodiment of the present invention;

FIG. **8**B is an illustration showing the metal **1** layer of FIG. **8**A with larger track widths for the metal **1** ground and power tracks, relative to the other metal **1** tracks;

FIG. **9** is an illustration showing a via **1** layer defined above and adjacent to the metal **1** layer of FIG. **8**A, in accordance with one embodiment of the present invention;

FIG. **10** is an illustration showing a metal **2** layer defined above and adjacent to the via **1** layer of FIG. **9**, in accordance with one embodiment of the present invention;

FIG. **11** is an illustration showing conductor tracks traversing the dynamic array in a first diagonal direction relative to the first and second reference directions (x) and (y), in accordance with one embodiment of the present invention;

FIG. **12** is an illustration showing conductor tracks traversing the dynamic array in a second diagonal direction relative to the first and second reference directions (x) and (y), in accordance with one embodiment of the present invention;

FIG. **13**A is an illustration showing an example of a sub-resolution contact layout used to lithographically reinforce diffusion contacts and gate electrode contacts, in accordance with one embodiment of the present invention;

FIG. **13**B is an illustration showing the sub-resolution contact layout of FIG. **13**A with sub-resolution contacts defined to fill the grid to the extent possible, in accordance with one embodiment of the present invention;

FIG. **13**C is an illustration showing an example of a sub-resolution contact layout utilizing various shaped sub-resolution contacts, in accordance with one embodiment of the present invention;

FIG. **13**D is an illustration showing an exemplary implementation of alternate phase shift masking (APSM) with sub-resolution contacts, in accordance with one embodiment of the present invention;

FIG. **14** is an illustration showing a semiconductor chip structure, in accordance with one embodiment of the present invention;

FIG. **14**A shows an annotated version of FIG. **14**;

FIG. **15** shows an example layout architecture defined in accordance with one embodiment of the present invention; and

FIG. **15**A shows an annotated version of FIG. **15**.

## DETAILED DESCRIPTION

In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one skilled in the art that the present invention may be practiced without some or all of these specific details. In other instances, well known process operations have not been described in detail in order not to unnecessarily obscure the present invention.

Generally speaking, a dynamic array architecture is provided to address semiconductor manufacturing process vari-

ability associated with a continually increasing lithographic gap. In the area of semiconductor manufacturing, lithographic gap is defined as the difference between the minimum size of a feature to be defined and the wavelength of light used to render the feature in the lithographic process, wherein the feature size is less than the wavelength of the light. Current lithographic processes utilize a light wavelength of 193 nm. However, current feature sizes are as small as 65 nm and are expected to soon approach sizes as small as 45 nm With a size of 65 nm, the shapes are three times smaller than the wavelength of the light used to define the shapes. Also, considering that the interaction radius of light is about five light wavelengths, it should be appreciated that shapes exposed with a 193 nm light source will influence the exposure of shapes approximately 5*193 nm (965 nm) away. When considering the 65 nm sized features with respect to 90 nm sized features, it should be appreciated that approximately two times as many 65 nm sizes features may be within the 965 nm interaction radius of the 193 nm light source as compared to the 90 nm sized features.

Due to the increased number of features within the interaction radius of the light source, the extent and complexity of light interference contributing to exposure of a given feature is significant. Additionally, the particular shapes associated with the features within the interaction radius of the light source weighs heavily on the type of light interactions that occur. Traditionally, designers were allowed to define essentially any two-dimensional topology of feature shapes so long as a set of design rules were satisfied. For example, in a given layer of the chip, i.e., in a given mask, the designer may have defined two-dimensionally varying features having bends that wrap around each other. When such two-dimensionally varying features are located in neighboring proximity to each other, the light used to expose the features will interact in a complex and generally unpredictable manner. The light interaction becomes increasingly more complex and unpredictable as the feature sizes and relative spacing become smaller.

Traditionally, if a designer follows the established set of design rules, the resulting product will be manufacturable with a specified probability associated with the set of design rules. Otherwise, for a design that violates the set of design rules, the probability of successful manufacture of the resulting product is unknown. To address the complex light interaction between neighboring two-dimensionally varying features, in the interest of successful product manufacturing, the set of design rules is expanded significantly to adequately address the possible combinations of two-dimensionally varying features. This expanded set of design rules quickly becomes so complicated and unwieldy that application of the expanded set of design rules becomes prohibitively time consuming, expensive, and prone to error. For example, the expanded set of design rules requires complex verification. Also, the expanded set of design rules may not be universally applied. Furthermore, manufacturing yield is not guaranteed even if all design rules are satisfied.

It should be appreciated that accurate prediction of all possible light interactions when rendering arbitrarily-shaped two-dimensional features is generally not feasible. Moreover, as an alternative to or in combination with expansion of the set of design rules, the set of design rules may also be modified to include increased margin to account for unpredictable light interaction between the neighboring two-dimensionally varying features. Because the design rules are established in an attempt to cover the random two-dimensional feature topology, the design rules may incorporate a significant amount of margin. While addition of margin in the set of design rules assists with the layout portions that include the neighboring two-dimensionally varying features, such global addition of margin causes other portions of the layout that do not include the neighboring two-dimensionally varying features to be overdesigned, thus leading to decreased optimization of chip area utilization and electrical performance.

In view of the foregoing, it should be appreciated that semiconductor product yield is reduced as a result of parametric failures that stem from variability introduced by design-dependent unconstrained feature topologies, i.e., arbitrary two-dimensionally varying features disposed in proximity to each other. By way of example, these parametric failures may result from failure to accurately print contacts and vias and from variability in fabrication processes. The variability in fabrication processes may include CMP dishing, layout feature shape distortion due to photolithography, gate distortion, oxide thickness variability, implant variability, and other fabrication related phenomena. The dynamic array architecture of the present invention is defined to address the above-mentioned semiconductor manufacturing process variability.

FIG. **1** is an illustration showing a number of neighboring layout features and a representation of light intensity used to render each of the layout features, in accordance with one embodiment of the present invention. Specifically, three neighboring linear-shaped layout features (**101**A-**101**C) are depicted as being disposed in a substantially parallel relationship within a given mask layer. The distribution of light intensity from a layout feature shape is represented by a sin c function. The sin c functions (**103**A-**103**C) represent the distribution of light intensity from each of the layout features (**101**A-**101**C, respectively). The neighboring linear-shaped layout features (**101**A-**101**C) are spaced apart at locations corresponding to peaks of the sin c functions (**103**A-**103**C). Thus, constructive interference between the light energy associated with the neighboring layout features (**101**A-**101**C), i.e., at the peaks of the sin c functions (**103**A-**103**C), serves to reinforce the exposure of the neighboring shapes (**101**A-**101**C) for the layout feature spacing illustrated. In accordance with the foregoing, the light interaction represented in FIG. **1** represents a synchronous case.

As illustrated in FIG. **1**, when linear-shaped layout features are defined in a regular repeating pattern at an appropriate spacing, constructive interference of the light energy associated with the various layout features serves to enhance the exposure of each layout feature. The enhanced exposure of the layout features provided by the constructive light interference can dramatically reduce or even eliminate a need to utilize optical proximity correction (OPC) and/or reticle enhancement technology (RET) to obtain sufficient rendering of the layout features.

A forbidden pitch, i.e., forbidden layout feature spacing, occurs when the neighboring layout features (**101**A-**101**C) are spaced such that peaks of the sin c function associated with one layout feature align with valleys of the sin c function associated with another layout feature, thus causing destructive interference of the light energy. The destructive interference of the light energy causes the light energy focused at a given location to be reduced. Therefore, to realize the beneficial constructive light interference associated with neighboring layout features, it is necessary to predict the layout feature spacing at which the constructive overlap of the sin c function peaks will occur. Predictable constructive overlap of the sin c function peaks and corresponding layout feature shape enhancement can be realized if the layout feature shapes are rectangular, near the same size, and are oriented in the same direction, as illustrated by the layout features (**101**A-**101**C) in FIG. **1**. In this manner, resonant light energy from neighbor-

ing layout feature shapes is used to enhance the exposure of a particular layout feature shape.

FIG. **2** is an illustration showing a generalized stack of layers used to define a dynamic array architecture, in accordance with one embodiment of the present invention. It should be appreciated that the generalized stack of layers used to define the dynamic array architecture, as described with respect to FIG. **2**, is not intended to represent an exhaustive description of the CMOS manufacturing process. However, the dynamic array is to be built in accordance with standard CMOS manufacturing processes. Generally speaking, the dynamic array architecture includes both the definition of the underlying structure of the dynamic array and the techniques for assembling the dynamic array for optimization of area utilization and manufacturability. Thus, the dynamic array is designed to optimize semiconductor manufacturing capabilities.

With regard to the definition of the underlying structure of the dynamic array, the dynamic array is built-up in a layered manner upon a base substrate **201**, e.g., upon a silicon substrate, or silicon-on-insulator (SOI) substrate. Diffusion regions **203** are defined in the base substrate **201**. The diffusion regions **203** represent selected regions of the base substrate **201** within which impurities are introduced for the purpose of modifying the electrical properties of the base substrate **201**. Above the diffusion regions **203**, diffusion contacts **205** are defined to enable connection between the diffusion regions **203** and conductor lines. For example, the diffusion contacts **205** are defined to enable connection between source and drain diffusion regions **203** and their respective conductor nets. Also, gate electrode features **207** are defined above the diffusion regions **203** to form transistor gates. Gate electrode contacts **209** are defined to enable connection between the gate electrode features **207** and conductor lines. For example, the gate electrode contacts **209** are defined to enable connection between transistor gates and their respective conductor nets.

Interconnect layers are defined above the diffusion contact **205** layer and the gate electrode contact layer **209**. The interconnect layers include a first metal (metal **1**) layer **211**, a first via (via **1**) layer **213**, a second metal (metal **2**) layer **215**, a second via (via **2**) layer **217**, a third metal (metal **3**) layer **219**, a third via (via **3**) layer **221**, and a fourth metal (metal **4**) layer **223**. The metal and via layers enable definition of the desired circuit connectivity. For example, the metal and via layers enable electrical connection of the various diffusion contacts **205** and gate electrode contacts **209** such that the logic function of the circuitry is realized. It should be appreciated that the dynamic array architecture is not limited to a specific number of interconnect layers, i.e., metal and via layers. In one embodiment, the dynamic array may include additional interconnect layers **225**, beyond the fourth metal (metal **4**) layer **223**. Alternatively, in another embodiment, the dynamic array may include less than four metal layers.

The dynamic array is defined such that layers (other than the diffusion region layer **203**) are restricted with regard to layout feature shapes that can be defined therein. Specifically, in each layer other than the diffusion region layer **203**, only linear-shaped layout features are allowed. A linear-shaped layout feature in a given layer is characterized as having a consistent vertical cross-section shape and extending in a single direction over the substrate. Thus, the linear-shaped layout features define structures that are one-dimensionally varying. The diffusion regions **203** are not required to be one-dimensionally varying, although they are allowed to be if necessary. Specifically, the diffusion regions **203** within the substrate can be defined to have any two-dimensionally varying shape with respect to a plane coincident with a top surface of the substrate. In one embodiment, the number of diffusion bend topologies is limited such that the interaction between the bend in diffusion and the conductive material, e.g., polysilicon, that forms the gate electrode of the transistor is predictable and can be accurately modeled. The linear-shaped layout features in a given layer are positioned to be parallel with respect to each other. Thus, the linear-shaped layout features in a given layer extend in a common direction over the substrate and parallel with the substrate.

The underlying layout methodology of the dynamic array uses constructive light interference of light waves in the lithographic process to reinforce exposure of neighboring shapes in a given layer. Therefore, the spacing of the parallel, linear-shaped layout features in a given layer is designed around the constructive light interference of the standing light waves such that lithographic correction (e.g., OPC/RET) is minimized or eliminated. Thus, in contrast to conventional OPC/RET-based lithographic processes, the dynamic array defined herein exploits the light interaction between neighboring features, rather than attempting to compensate for the light interaction between neighboring features.

Because the standing light wave for a given linear-shaped layout feature can be accurately modeled, it is possible to predict how the standing light waves associated with the neighboring linear-shaped layout features disposed in parallel in a given layer will interact. Therefore, it is possible to predict how the standing light wave used to expose one linear-shaped feature will contribute to the exposure of its neighboring linear-shaped features. Prediction of the light interaction between neighboring linear-shaped features enables the identification of an optimum feature-to-feature spacing such that light used to render a given shape will reinforce its neighboring shapes. The feature-to-feature spacing in a given layer is defined as the feature pitch, wherein the pitch is the center-to-center separation distance between adjacent linear-shaped features in a given layer.

To provide the desired exposure reinforcement between neighboring features, the linear-shaped layout features in a given layer are spaced such that constructive and destructive interference of the light from neighboring features will be optimized to produce the best rendering of all features in the neighborhood. The feature-to-feature spacing in a given layer is proportional to the wavelength of the light used to expose the features. The light used to expose each feature within about a five light wavelength distance from a given feature will serve to enhance the exposure of the given feature to some extent. The exploitation of constructive interference of the standing light waves used to expose neighboring features enables the manufacturing equipment capability to be maximized and not be limited by concerns regarding light interactions during the lithography process.

As discussed above, the dynamic array incorporates a restricted topology in which the features within each layer (other than diffusion) are required to be linear-shaped features that are oriented in a parallel manner to traverse over the substrate in a common direction. With the restricted topology of the dynamic array, the light interaction in the photolithography process can be optimized such that the printed image on the mask is essentially identical to the drawn shape in the layout, i.e., essentially a 100% accurate transfer of the layout onto the resist is achieved.

FIG. **3**A is an illustration showing an exemplary base grid to be projected onto the dynamic array to facilitate definition of the restricted topology, in accordance with one embodiment of the present invention. The base grid can be used to facilitate parallel placement of the linear-shaped features in

each layer of the dynamic array at the appropriate optimized pitch. Although not physically defined as part of the dynamic array, the base grid can be considered as a projection on each layer of the dynamic array. Also, it should be understood that the base grid is projected in a substantially consistent manner with respect to position on each layer of the dynamic array, thus facilitating accurate feature stacking and alignment.

In the exemplary embodiment of FIG. **3**A, the base grid is defined as a rectangular grid, i.e., Cartesian grid, in accordance with a first reference direction (x) and a second reference direction (y). The gridpoint-to-gridpoint spacing in the first and second reference directions can be defined as necessary to enable definition of the linear-shaped features at the optimized feature-to-feature spacing. Also, the gridpoint spacing in the first reference direction (x) can be different than the gridpoint spacing in the second reference direction (y). In one embodiment, a single base grid is projected across the entire die to enable location of the various linear-shaped features in each layer across the entire die. However, in other embodiments, separate base grids can be projected across separate regions of the die to support different feature-to-feature spacing requirements within the separate regions of the die. FIG. **3**B is an illustration showing separate base grids projected across separate regions of the die, in accordance with an exemplary embodiment of the present invention.

The base grid is defined with consideration for the light interaction function, i.e., the sin c function, and the manufacturing capability, wherein the manufacturing capability is defined by the manufacturing equipment and processes to be utilized in fabricating the dynamic array. With regard to the light interaction function, the base grid is defined such that the spacing between gridpoints enables alignment of peaks in the sin c functions describing the light energy projected upon neighboring gridpoints. Therefore, linear-shaped features optimized for lithographic reinforcement can be specified by drawing a line from a first gridpoint to a second gridpoint, wherein the line represents a rectangular structure of a given width. It should be appreciated that the various linear-shaped features in each layer can be specified according to their endpoint locations on the base grid and their width.

FIG. **3**C is an illustration showing an exemplary linear-shaped feature **301** defined to be compatible with the dynamic array, in accordance with one embodiment of the present invention. The linear-shaped feature **301** has a substantially rectangular cross-section defined by a width **303** and a height **307**. The linear-shaped feature **301** extends in a linear direction to a length **305**. In one embodiment, a cross-section of the linear-shaped feature, as defined by its width **303** and height **307**, is substantially uniform along its length **305**. It should be understood, however, that lithographic effects may cause a rounding of the ends of the linear-shaped feature **301**. The first and second reference directions (x) and (y), respectively, of FIG. **3**A are shown to illustrate an exemplary orientation of the linear-shaped feature on the dynamic array. It should be appreciated that the linear-shaped feature may be oriented to have its length **305** extend in either the first reference direction (x), the second reference direction (y), or in diagonal direction defined relative to the first and second reference directions (x) and (y). Regardless of the linear-shaped features' particular orientation with respect to the first and second reference directions (x) and (y), it should be understood that the linear-shaped feature is defined in a plane that is substantially parallel to a top surface of the substrate upon which the dynamic array is built. Also, it should be understood that the linear-shaped feature is free of bends, i.e., change in direction, in the plane defined by the first and second reference directions.

FIG. **3**D is an illustration showing another exemplary linear-shaped feature **317** defined to be compatible with the dynamic array, in accordance with one embodiment of the present invention. The linear-shaped feature **317** has a trapezoidal cross-section defined by a lower width **313**, an upper width **315**, and a height **309**. The linear-shaped feature **317** extends in a linear direction to a length **311**. In one embodiment, the cross-section of the linear-shaped feature **317** is substantially uniform along its length **311**. It should be understood, however, that lithographic effects may cause a rounding of the ends of the linear-shaped feature **317**. The first and second reference directions (x) and (y), respectively, of FIG. **3**A are shown to illustrate an exemplary orientation of the linear-shaped feature on the dynamic array. It should be appreciated that the linear-shaped feature **317** may be oriented to have its length **311** extend in either the first reference direction (x), the second reference direction (y), or in diagonal direction defined relative to the first and second reference directions (x) and (y). Regardless of the particular orientation of the linear-shaped feature **317** with regard to the first and second reference directions (x) and (y), it should be understood that the linear-shaped feature **317** is defined in a plane that is substantially parallel to a top surface of the substrate upon which the dynamic array is built. Also, it should be understood that the linear-shaped feature **317** is free of bends, i.e., change in direction, in the plane defined by the first and second reference directions.

Although FIGS. **3**C and **3**D explicitly discuss linear shaped features having rectangular and trapezoidal cross-sections, respectively, it should be understood that the linear shaped features having other types of cross-sections can be defined within the dynamic array. Therefore, essentially any suitable cross-sectional shape of the linear-shaped feature can be utilized so long as the linear-shaped feature is defined to have a length that extends in one direction, and is oriented to have its length extend in either the first reference direction (x), the second reference direction (y), or in diagonal direction defined relative to the first and second reference directions (x) and (y).

The layout architecture of the dynamic array follows the base grid pattern. Thus, it is possible to use grid points to represent where changes in direction occur in diffusion, wherein gate electrode and metal linear-shaped features are placed, where contacts are placed, where opens are in the linear-shaped gate electrode and metal features, etc. The pitch of the gridpoints, i.e., the gridpoint-to-gridpoint spacing, should be set for a given feature line width, e.g., width **303** in FIG. **3**C, such that exposure of neighboring linear-shaped features of the given feature line width will reinforce each other, wherein the linear-shaped features are centered on gridpoints. With reference to the dynamic array stack of FIG. **2** and the exemplary base grid of FIG. **3**A, in one embodiment, the gridpoint spacing in the first reference direction (x) is set by the required gate electrode gate pitch. In this same embodiment, the gridpoint pitch in the second reference direction (y) is set by the metal **1** and metal **3** pitch. For example, in a 90 nm process technology, i.e., minimum feature size equal to 90 nm, the gridpoint pitch in the second reference direction (y) is about 0.24 micron. In one embodiment, metal **1** and metal **2** layers will have a common spacing and pitch. A different spacing and pitch may be used above the metal **2** layer.

The various layers of the dynamic array are defined such that the linear-shaped features in adjacent layers extend in a crosswise manner with respect to each other. For example, the linear-shaped features of adjacent layers may extend orthogonally, i.e., perpendicularly with respect to each other. Also, the linear-shaped features of one layer may extend across the

linear-shaped features of an adjacent layer at an angle, e.g., at about 45 degrees. For example, in one embodiment the linear-shaped feature of one layer extend in the first reference direction (x) and the linear-shaped features of the adjacent layer extend diagonally with respect to the first (x) and second (y) reference directions. It should be appreciated that to route a design in the dynamic array having the linear-shaped features positioned in the crosswise manner in adjacent layers, opens can be defined in the linear-shaped features, and contacts and vias can be defined as necessary.

The dynamic array minimizes the use of bends in layout shapes to eliminate unpredictable lithographic interactions. Specifically, prior to OPC or other RET processing, the dynamic array allows bends in the diffusion layer to enable control of device sizes, but does not allow bends in layers above the diffusion layer. The layout features in each layer above the diffusion layer are linear in shape, e.g., FIG. **3**C, and disposed in a parallel relationship with respect to each other. The linear shapes and parallel positioning of layout features are implemented in each stack layer of the dynamic array where predictability of constructive light interference is necessary to ensure manufacturability. In one embodiment, the linear shapes and parallel positioning of layout features are implemented in the dynamic array in each layer above diffusion through metal **2**. Above metal **2**, the layout features may be of sufficient size and shape that constructive light interference is not required to ensure manufacturability. However, the presence of constructive light interference in patterning layout features above metal **2** may be beneficial.

An exemplary buildup of dynamic array layers from diffusion through metal **2** are described with respect to FIGS. **4** through **14**. It should be appreciated that the dynamic array described with respect to FIGS. **4** through **14** is provided by way of example only, and is not intended to convey limitations of the dynamic array architecture. The dynamic array can be used in accordance with the principles presented herein to define essentially any integrated circuit design.

FIG. **4** is an illustration showing a diffusion layer layout of an exemplary dynamic array, in accordance with one embodiment of the present invention. The diffusion layer of FIG. **4** shows a p-diffusion region **401** and an n-diffusion region **403**. While the diffusion regions are defined according to the underlying base grid, the diffusion regions are not subject to the linear-shaped feature restrictions associated with the layers above the diffusion layer. The diffusion regions **401** and **403** include diffusion squares **405** defined where diffusion contacts will be located. The diffusion regions **401** and **403** do not include extraneous jogs or corners, thus improving the use of lithographic resolution and enabling more accurate device extraction. Additionally, n+ mask regions (**412** and **416**) and p+ mask regions (**410** and **414**) are defined as rectangles on the (x), (y) grid with no extraneous jogs or notches. This style permits use of larger diffusion regions, eliminates need for OPC/RET, and enables use of lower resolution and lower cost lithographic systems, e.g., i-line illumination at 365 nm. It should be appreciated that the n+ mask region **416** and the p+ mask region **410**, as depicted in FIG. **4**, are for an embodiment that does not employ well-biasing. In an alternative embodiment where well-biasing is to be used, the n+ mask region **416** shown in FIG. **4** will actually be defined as a p+ mask region. Also, in this alternative embodiment, the p+ mask region **410** shown in FIG. **4** will actually be defined as a n+ mask region.

FIG. **5** is an illustration showing a gate electrode layer and a diffusion contact layer above and adjacent to the diffusion layer of FIG. **4**, in accordance with one embodiment of the present invention. As those skilled in the CMOS arts will appreciate, the gate electrode features **501** define the transistor gates. The gate electrode features **501** are defined as linear shaped features extending in a parallel relationship across the dynamic array in the second reference direction (y). In one embodiment, the gate electrode features **501** are defined to have a common width. However, in another embodiment, one or more of the gate electrode features can be defined to have a different width. For example, FIG. **5** shows a gate electrode features **501**A that has a larger width relative to the other gate electrode features **501**. The pitch (center-to-center spacing) of the gate electrode features **501** is minimized while ensuring optimization of lithographic reinforcement, i.e., resonant imaging, provided by neighboring gate electrode features **501**. For discussion purposes, gate electrode features **501** extending across the dynamic array in a given line are referred to as a gate electrode track.

The gate electrode features **501** form n-channel and p-channel transistors as they cross the diffusion regions **403** and **401**, respectively. Optimal gate electrode feature **501** printing is achieved by drawing gate electrode features **501** at every grid location, even though no diffusion region may be present at some grid locations. Also, long continuous gate electrode features **501** tend to improve line end shortening effects at the ends of gate electrode features within the interior of the dynamic array. Additionally, gate electrode printing is significantly improved when all bends are removed from the gate electrode features **501**.

Each of the gate electrode tracks may be interrupted, i.e., broken, any number of times in linearly traversing across the dynamic array in order to provide required electrical connectivity for a particular logic function to be implemented. When a given gate electrode track is required to be interrupted, the separation between ends of the gate electrode track segments at the point of interruption is minimized to the extent possible taking into consideration the manufacturing capability and electrical effects. In one embodiment, optimal manufacturability is achieved when a common end-to-end spacing is used between features within a particular layer.

Minimizing the separation between ends of the gate electrode track segments at the points of interruption serves to maximize the lithographic reinforcement, and uniformity thereof, provided from neighboring gate electrode tracks. Also, in one embodiment, if adjacent gate electrode tracks need to be interrupted, the interruptions of the adjacent gate electrode tracks are made such that the respective points of interruption are offset from each other so as to avoid, to the extent possible, an occurrence of neighboring points of interruption. More specifically, points of interruption within adjacent gate electrode tracks are respectively positioned such that a line of sight does not exist through the points of interruption, wherein the line of sight is considered to extend perpendicularly to the direction in which the gate electrode tracks extend over the substrate. Additionally, in one embodiment, the gate electrodes may extend through the boundaries at the top and bottom of the cells, i.e., the PMOS or NMOS cells. This embodiment would enable bridging of neighboring cells.

With further regard to FIG. **5**, diffusion contacts **503** are defined at each diffusion square **405** to enhance the printing of diffusion contacts via resonant imaging. The diffusion squares **405** are present around every diffusion contact **503** to enhance the printing of the power and ground connection polygons at the diffusion contacts **503**.

The gate electrode features **501** and diffusion contacts **503** share a common grid spacing. More specifically, the gate electrode feature **501** placement is offset by one-half the grid spacing relative to the diffusion contacts **503**. For example, if the gate electrode features **501** and diffusion contact **503** grid

spacing is 0.36 μm, then the diffusion contacts are placed such that the x-coordinate of their center falls on an integer multiple of 0.36 μm, while the x-coordinate of the center of each gate electrode feature **501** minus 0.18 μm should be an integer multiple of 0.36 μm. In the present example, the x-coordinates are represented by the following:

Diffusion contact center x-coordinate=I*0.36 μm, where I is the grid number;

Gate electrode feature center x-coordinate=0.18 μm+I*0.36 μm, where I is the grid number.

The grid based system of the dynamic array ensures that all contacts (diffusion and gate electrode) will land on a horizontal grid that is equal to a multiple of one-half of the diffusion contact grid and a vertical grid that is set by the metal **1** pitch. In the example above, the gate electrode feature and diffusion contact grid is 0.36 μm. The diffusion contacts and gate electrode contacts will land on a horizontal grid that is a multiple of 0.18 μm. Also, the vertical grid for 90 nm process technologies is about 0.24 μm.

FIG. **6** is an illustration showing a gate electrode contact layer defined above and adjacent to the gate electrode layer of FIG. **5**, in accordance with one embodiment of the present invention. In the gate electrode contact layer, gate electrode contacts **601** are drawn to enable connection of the gate electrode features **501** to the overlying metal conduction lines. In general, design rules will dictate the optimum placement of the gate electrode contacts **601**. In one embodiment, the gate electrode contacts are drawn on top of the transistor endcap regions. This embodiment minimizes white space in the dynamic array when design rules specify long transistor endcaps. In some process technologies white space may be minimized by placing a number of gate electrode contacts for a cell in the center of the cell. Also, it should be appreciated that in the present invention, the gate electrode contact **601** is oversized in the direction perpendicular to the gate electrode feature **501** to ensure overlap between the gate electrode contact **601** and the gate electrode feature **501**.

FIG. **6**A shows an annotated version of FIG. **6**. The features depicted in FIG. **6**A are exactly the same as the features depicted in FIG. **6**. FIG. **6**A shows a first conductive gate level structure **501***a* having a lengthwise centerline **6***a***01**. FIG. **6**A shows a second conductive gate level structure **501***b* and a third conductive gate level structure **501***c* having a lengthwise centerline **6***a***03**. FIG. **6**A shows a fourth conductive gate level structure **501***d* and a fifth conductive gate level structure **501***e* having the lengthwise centerline **6***a***05**. FIG. **6**A shows a sixth conductive gate level structure **501***f* having a lengthwise centerline **6***a***07**. FIG. **6**A shows a seventh conductive gate level structure **501***g* having a lengthwise centerline **6***a***09**. FIG. **6**A shows an eighth conductive gate level structure **501***h* having a lengthwise centerline **6***a***11**.

FIG. **6**A shows the first conductive gate level structure **501***a* separated from each of the second conductive gate level structure **501***b* and third conductive gate level structure **501***c* by a centerline-to-centerline spacing **6***a***13** as measured in a direction perpendicular to the parallel direction of the gate level structures. FIG. **6**A shows the second conductive gate level structure **501***b* separated from the fourth conductive gate level structure **501***d* by a centerline-to-centerline spacing **6***a***15** as measured in the direction perpendicular to the parallel direction of the gate level structures. FIG. **6**A shows the third conductive gate level structure **501***c* separated from the fifth conductive gate level structure **501***e* by a centerline-to-centerline spacing **6***a***15** as measured in the direction perpendicular to the parallel direction of the gate level structures. FIG. **6**A shows the sixth conductive gate level structure **501***f* separated from each of the fourth conductive gate level structure **501***d* and fifth conductive gate level structure **501***e* by a centerline-to-centerline spacing **6***a***17** as measured in the direction perpendicular to the parallel direction of the gate level structures. FIG. **6**A shows the sixth conductive gate level structure **501***f* separated from the seventh conductive gate level structure **501***g* by a centerline-to-centerline spacing **6***a***19** as measured in the direction perpendicular to the parallel direction of the gate level structures. FIG. **6**A shows the seventh conductive gate level structure **501***g* separated from the eighth conductive gate level structure **501***h* by a centerline-to-centerline spacing **6***a***21** as measured in the direction perpendicular to the parallel direction of the gate level structures.

FIG. **6**A shows the first conductive gate level structure **501***a* forming a gate electrode of a transistor **6***a***47** of a first transistor type and a gate electrode of a transistor **6***a***37** of a second transistor type. FIG. **6**A shows the second conductive gate level structure **501***b* forming a gate electrode of a transistor **6***a***49** of the first transistor type. FIG. **6**A shows the third conductive gate level structure **501***c* forming a gate electrode of a transistor **6***a***39** of the second transistor type. FIG. **6**A shows the fourth conductive gate level structure **501***d* forming a gate electrode of a transistor **6***a***51** of the first transistor type. FIG. **6**A shows the fifth conductive gate level structure **501***e* forming a gate electrode of a transistor **6***a***41** of the second transistor type. FIG. **6**A shows the sixth conductive gate level structure **501***f* forming a gate electrode of a transistor **6***a***53** of the first transistor type and a gate electrode of a transistor **6***a***43** of the second transistor type. FIG. **6**A shows the seventh conductive gate level structure **501***g* not forming a gate electrode of a transistor. FIG. **6**A shows the eighth conductive gate level structure **501***h* forming a gate electrode of a transistor **6***a***55** of the first transistor type and a gate electrode of a transistor **6***a***45** of the second transistor type.

FIG. **6**A shows the contact **601***a* connected to the first conductive gate level structure **501***a*. FIG. **6**A shows the contact **601***b* connected to the second conductive gate level structure **501***b*. FIG. **6**A shows the contact **601***c* connected to the third conductive gate level structure **501***c*. FIG. **6**A shows the contact **601***d* connected to the fourth conductive gate level structure **501***d*. FIG. **6**A shows the contact **601***e* connected to the fifth conductive gate level structure **501***e*. FIG. **6**A shows the contact **601***f* connected to the sixth conductive gate level structure **501***f*.

FIG. **6**A shows the contact **601***b* positioned to contact the second conductive gate level structure **501***b* at a contact-to-gate distance **6***a***25** from a gate electrode of the transistor **6***a***49**. FIG. **6**A shows the contact **601***c* positioned to contact the third conductive gate level structure **501***c* at a contact-to-gate distance **6***a***27** from a gate electrode of the transistor **6***a***39**. FIG. **6**A shows the contact **601***d* positioned to contact the fourth conductive gate level structure **501***d* at a contact-to-gate distance **6***a***23** from a gate electrode of the transistor **6***a***51**. FIG. **6**A shows the contact **601***e* positioned to contact the fifth conductive gate level structure **501***e* at a contact-to-gate distance **6***a***29** from a gate electrode of the transistor **6***a***41**.

FIG. **6**B shows an annotated version of FIG. **6**. The features depicted in FIG. **6**B are exactly the same as the features depicted in FIG. **6**. FIG. **6**B shows the contact **601***b* located at a contact position **6***a***31** in the parallel direction of the conductive gate level structures, i.e., in the y direction. FIG. **6**B shows the contact **601***c* and the contact **601***d* located at a contact position **6***a***33** in the parallel direction of the conductive gate level structures. FIG. **6**B shows the contact **601***e* located at a contact position **6***a***35** in the parallel direction of the conductive gate level structures. FIG. **6**B shows the con-

tacts **601***b* and **601***e* positioned outside the diffusion regions **401** and **403** of different diffusion region types. FIG. **6**B shows the contacts **601***c* and **601***d* positioned between the diffusion regions **401** and **403** of different diffusion region types, i.e., positioned over the inner non-diffusion region between the diffusion regions **401** and **403** of different diffusion region types.

FIG. **6**C shows an annotated version of FIG. **6**. The features depicted in FIG. **6**C are exactly the same as the features depicted in FIG. **6**. FIG. **6**C shows the second conductive gate level structure **501***b* extending a distance **6***a***57** beyond the contact **601***b* in the parallel direction (y-direction) away from the gate electrode of the transistor **6***a***49**. FIG. **6**C shows the third conductive gate level structure **501***c* extending a distance **6***a***59** beyond the contact **601***c* in the parallel direction (y-direction) away from the gate electrode of the transistor **6***a***39**. FIG. **6**C shows the fourth conductive gate level structure **501***d* extending a distance **6***a***61** beyond the contact **601***d* in the parallel direction (y-direction) away from the gate electrode of the transistor **6***a***51**. FIG. **6**C shows the fifth conductive gate level structure **501***e* extending a distance **6***a***63** beyond the contact **601***e* in the parallel direction (y-direction) away from the gate electrode of the transistor **6***a***41**.

FIG. **6**D shows an annotated version of FIG. **6**. The features depicted in FIG. **6**D are exactly the same as the features depicted in FIG. **6**. FIG. **6**D shows the first conductive gate level structure **501***a* defined to have a length **6***a***89** as measured in the parallel direction (y-direction). FIG. **6**D shows the second conductive gate level structure **501***b* defined to have a length **6***a***93** as measured in the parallel direction (y-direction). FIG. **6**D shows the third conductive gate level structure **501***c* defined to have a length **6***a***91** as measured in the parallel direction (y-direction). FIG. **6**D shows the fourth conductive gate level structure **501***d* defined to have a length **6***a***97** as measured in the parallel direction (y-direction). FIG. **6**D shows the fifth conductive gate level structure **501***e* defined to have a length **6***a***95** as measured in the parallel direction (y-direction). FIG. **6**D shows the sixth conductive gate level structure **501***f* defined to have a length **6***a***99** as measured in the parallel direction (y-direction). FIG. **6**D shows the seventh conductive gate level structure **501***g* defined to have a length **6***a***101** as measured in the parallel direction (y-direction). FIG. **6**D shows the eighth conductive gate level structure **501***h* defined to have a length **6***a***103** as measured in the parallel direction (y-direction).

FIG. **6**D shows the second conductive gate level structure **501***b* positioned in a spaced apart end-to-end manner with the third conductive gate level structure **501***c*. FIG. **6**D shows the second conductive gate level structure **501***b* separated from the third conductive gate level structure **501***c* by a first end-to-end spacing **6***a***85** as measured in the parallel direction (y-direction). FIG. **6**D shows the fourth conductive gate level structure **501***d* positioned in a spaced apart end-to-end manner with the fifth conductive gate level structure **501***e*. FIG. **6**D shows the fourth conductive gate level structure **501***d* separated from the fifth conductive gate level structure **501***e* by a second end-to-end spacing **6***a***87** as measured in the parallel direction (y-direction). FIG. **6**D shows the first end-to-end spacing **6***a***85** positioned over the inner non-diffusion region between the two diffusion regions **401** and **403** of different diffusion types. FIG. **6**D shows the second end-to-end spacing **6***a***87** positioned over the inner non-diffusion region between the two diffusion regions **401** and **403** of different diffusion types. FIG. **6**D shows the first end-to-end spacing **6***a***85** offset in the parallel direction (y-direction) from the second end-to-end spacing **6***a***87**.

FIG. **6**D shows the first, second, fourth, sixth, seventh, and eighth conductive gate level structures **501***a*, **501***b*, **501***d*, **501***f*, **501***g*, **501***h*, respectively, each having an end aligned with a first common position **6***a***81** in the parallel direction (y-direction). FIG. **6**D shows the first, third, fifth, sixth, seventh, and eighth conductive gate level structures **501***a*, **501***c*, **501***e*, **501***f*, **501***g*, **501***h*, respectively, each having an end aligned with a second common position **6***a***83** in the parallel direction (y-direction).

FIG. **6**E shows an annotated version of FIG. **6**. The features depicted in FIG. **6**E are exactly the same as the features depicted in FIG. **6**. FIG. **6**E shows the second conductive gate level feature **501***b* having an outer extension distance **6***a***105** as measured in the parallel direction (y-direction) away from the gate electrode of the transistor **6***a***49** and away from the transistor **6***a***39**. FIG. **6**E shows the second conductive gate level feature **501***b* having an inner extension distance **6***a***107** as measured in the parallel direction (y-direction) away from the gate electrode of the transistor **6***a***49** and toward the transistor **6***a***39**. FIG. **6**E shows the third conductive gate level feature **501***c* having an outer extension distance **6***a***111** as measured in the parallel direction (y-direction) away from the gate electrode of the transistor **6***a***39** and away from the transistor **6***a***49**. FIG. **6**E shows the third conductive gate level feature **501***c* having an inner extension distance **6***a***109** as measured in the parallel direction (y-direction) away from the gate electrode of the transistor **6***a***39** and toward the transistor **6***a***49**.

FIG. **6**E shows the fourth conductive gate level feature **501***d* having an outer extension distance **6***a***113** as measured in the parallel direction (y-direction) away from the gate electrode of the transistor **6***a***51** and away from the transistor **6***a***41**. FIG. **6**E shows the fourth conductive gate level feature **501***d* having an inner extension distance **6***a***115** as measured in the parallel direction (y-direction) away from the gate electrode of the transistor **6***a***51** and toward the transistor **6***a***41**. FIG. **6**E shows the fifth conductive gate level feature **501***e* having an outer extension distance **6***a***119** as measured in the parallel direction (y-direction) away from the gate electrode of the transistor **6***a***41** and away from the transistor **6***a***51**. FIG. **6**E shows the fifth conductive gate level feature **501***e* having an inner extension distance **6***a***117** as measured in the parallel direction (y-direction) away from the gate electrode of the transistor **6***a***41** and toward the transistor **6***a***51**. FIG. **7**A is an illustration showing a traditional approach for making contact to a gate electrode, e.g., polysilicon feature. In the traditional configuration of FIG. **7**A, an enlarged rectangular gate electrode region **707** is defined where a gate electrode contact **709** is to be located. The enlarged rectangular gate electrode region **707** introduces a bend of distance **705** in the gate electrode. The bend associated with the enlarged rectangular gate electrode region **707** sets up undesirable light interactions and distorts the gate electrode line **711**. Distortion of the gate electrode line **711** is especially problematic when the gate electrode width is about the same as a transistor length.

FIG. **7**B is an illustration showing a gate electrode contact **601**, e.g., polysilicon contact, defined in accordance with one embodiment of the present invention. The gate electrode contact **601** is drawn to overlap the edges of the gate electrode feature **501**, and extend in a direction substantially perpendicular to the gate electrode feature **501**. In one embodiment, the gate electrode contact **601** is drawn such that the vertical dimension **703** is same as the vertical dimension used for the diffusion contacts **503**. For example, if the diffusion contact **503** opening is specified to be 0.12 μm square then the vertical dimension of the gate electrode contact **601** is drawn at 0.12

μm. However, in other embodiments, the gate electrode contact **601** can be drawn such that the vertical dimension **703** is different from the vertical dimension used for the diffusion contacts **503**.

In one embodiment, the gate electrode contact **601** extension **701** beyond the gate electrode feature **501** is set such that maximum overlap is achieved between the gate electrode contact **601** and the gate electrode feature **501**. The extension **701** is defined to accommodate line end shortening of the gate electrode contact **601**, and misalignment between the gate electrode contact layer and gate electrode feature layer. The length of the gate electrode contact **601** is defined to ensure maximum surface area contact between the gate electrode contact **601** and the gate electrode feature **501**, wherein the maximum surface area contact is defined by the width of the gate electrode feature **501**.

FIG. **8**A is an illustration showing a metal **1** layer defined above the gate electrode contact layer of FIG. **6**, in accordance with one embodiment of the present invention. The metal **1** layer includes a number of metal **1** tracks **801-821** defined to include linear shaped features extending in a parallel relationship across the dynamic array. The metal **1** tracks **801-821** extend in a direction substantially perpendicular to the gate electrode features **501** in the underlying gate electrode layer of FIG. **5**. Thus, in the present example, the metal **1** tracks **801-821** extend linearly across the dynamic array in the first reference direction (x). The pitch (center-to-center spacing) of the metal **1** tracks **801-821** is minimized while ensuring optimization of lithographic reinforcement, i.e., resonant imaging, provided by neighboring metal **1** tracks **801-821**. For example, in one embodiment, the metal **1** tracks **801-821** are centered on a vertical grid of about 0.24 μm for a 90 nm process technology.

Each of the metal **1** tracks **801-821** may be interrupted, i.e., broken, any number of times in linearly traversing across the dynamic array in order to provide required electrical connectivity for a particular logic function to be implemented. When a given metal **1** track **801-821** is required to be interrupted, the separation between ends of the metal **1** track segments at the point of interruption is minimized to the extent possible taking into consideration manufacturing capability and electrical effects. Minimizing the separation between ends of the metal **1** track segments at the points of interruption serves to maximize the lithographic reinforcement, and uniformity thereof, provided from neighboring metal **1** tracks. Also, in one embodiment, if adjacent metal **1** tracks need to be interrupted, the interruptions of the adjacent metal **1** tracks are made such that the respective points of interruption are offset from each other so as to avoid, to the extent possible, an occurrence of neighboring points of interruption. More specifically, points of interruption within adjacent metal **1** tracks are respectively positioned such that a line of sight does not exist through the points of interruption, wherein the line of sight is considered to extend perpendicularly to the direction in which the metal **1** tracks extend over the substrate.

In the example of FIG. **8**A, the metal **1** track **801** is connected to the ground supply, and the metal **1** track **821** is connected to the power supply voltage. In the embodiment of FIG. **8**A, the widths of the metal **1** tracks **801** and **821** are the same as the other metal **1** tracks **803-819**. However, in another embodiment, the widths of metal **1** tracks **801** and **821** are larger than the widths of the other metal **1** tracks **803-819**. FIG. **8**B is an illustration showing the metal **1** layer of FIG. **8**A with larger track widths for the metal **1** ground and power tracks (**801**A and **821**A), relative to the other metal **1** tracks **803-819**.

The metal **1** track pattern is optimally configured to optimize the use of "white space" (space not occupied by transistors). The example of FIG. **8**A includes the two shared metal **1** power tracks **801** and **821**, and nine metal **1** signal tracks **803-819**. Metal **1** tracks **803**, **809**, **811**, and **819** are defined as gate electrode contact tracks in order to minimize white space. Metal **1** tracks **805** and **807** are defined to connect to n-channel transistor source and drains. Metal **1** tracks **813**, **815**, and **817** are defined to connect to p-channel source and drains. Also, any of the nine metal **1** signal tracks **803-819** can be used as a feed through if no connection is required. For example, metal **1** tracks **813** and **815** are configured as feed through connections.

FIG. **9** is an illustration showing a via **1** layer defined above and adjacent to the metal **1** layer of FIG. **8**A, in accordance with one embodiment of the present invention. Vias **901** are defined in the via **1** layer to enable connection of the metal **1** tracks **801-821** to higher level conduction lines.

FIG. **10** is an illustration showing a metal **2** layer defined above and adjacent to the via **1** layer of FIG. **9**, in accordance with one embodiment of the present invention. The metal **2** layer includes a number of metal **2** tracks **1001** defined as linear shaped features extending in a parallel relationship across the dynamic array. The metal **2** tracks **1001** extend in a direction substantially perpendicular to the metal **1** tracks **801-821** in the underlying metal **1** layer of FIG. **8**A, and in a direction substantially parallel to the gate electrode tracks **501** in the underlying gate electrode layer of FIG. **5**. Thus, in the present example, the metal **2** tracks **1001** extend linearly across the dynamic array in the second reference direction (y).

The pitch (center-to-center spacing) of the metal **2** tracks **1001** is minimized while ensuring optimization of lithographic reinforcement, i.e., resonant imaging, provided by neighboring metal **2** tracks. It should be appreciated that regularity can be maintained on higher level interconnect layers in the same manner as implemented in the gate electrode and metal **1** layers. In one embodiment, the gate electrode feature **501** pitch and the metal **2** track pitch is the same. In another embodiment, the contacted gate electrode pitch (e.g., polysilicon-to-polysilicon space with a diffusion contact in between) is greater than the metal **2** track pitch. In this embodiment, the metal **2** track pitch is optimally set to be ⅔ or ¾ of the contacted gate electrode pitch. Thus, in this embodiment, the gate electrode track and metal **2** track align at every two gate electrode track pitches and every three metal **2** track pitches. For example, in a 90 nm process technology, the optimum contacted gate electrode track pitch is 0.36 μm, and the optimum metal **2** track pitch is 0.24 μm. In another embodiment, the gate electrode track and the metal **2** track align at every three gate electrode pitches and every four metal **2** pitches. For example, in a 90 nm process technology, the optimum contacted gate electrode track pitch is 0.36 μm, and the optimum metal **2** track pitch is 0.27 μm.

Each of the metal **2** tracks **1001** may be interrupted, i.e., broken, any number of times in linearly traversing across the dynamic array in order to provide required electrical connectivity for a particular logic function to be implemented. When a given metal **2** track **1001** is required to be interrupted, the separation between ends of the metal **2** track segments at the point of interruption is minimized to the extent possible taking into consideration manufacturing and electrical effects. Minimizing the separation between ends of the metal **2** track segments at the points of interruption serves to maximize the lithographic reinforcement, and uniformity thereof, provided from neighboring metal **2** tracks. Also, in one embodiment, if adjacent metal **2** tracks need to be interrupted, the interrup-

tions of the adjacent metal **2** tracks are made such that the respective points of interruption are offset from each other so as to avoid, to the extent possible, an occurrence of neighboring points of interruption. More specifically, points of interruption within adjacent metal **2** tracks are respectively positioned such that a line of sight does not exist through the points of interruption, wherein the line of sight is considered to extend perpendicularly to the direction in which the metal **2** tracks extend over the substrate.

As discussed above, the conduction lines in a given metal layer above the gate electrode layer may traverse the dynamic array in a direction coincident with either the first reference direction (x) or the second reference direction (y). It should be further appreciated that the conduction lines in a given metal layer above the gate electrode layer may traverse the dynamic array in a diagonal direction relative to the first and second reference directions (x) and (y). FIG. **11** is an illustration showing conductor tracks **1101** traversing the dynamic array in a first diagonal direction relative to the first and second reference directions (x) and (y), in accordance with one embodiment of the present invention. FIG. **12** is an illustration showing conductor tracks **1201** traversing the dynamic array in a second diagonal direction relative to the first and second reference directions (x) and (y), in accordance with one embodiment of the present invention.

As with the metal **1** and metal **2** tracks discussed above, the diagonal traversing conductor tracks **1101** and **1201** of FIGS. **11** and **12** may be interrupted, i.e., broken, any number of times in linearly traversing across the dynamic array in order to provide required electrical connectivity for a particular logic function to be implemented. When a given diagonal traversing conductor track is required to be interrupted, the separation between ends of the diagonal conductor track at the point of interruption is minimized to the extent possible taking into consideration manufacturing and electrical effects. Minimizing the separation between ends of the diagonal conductor track at the points of interruption serves to maximize the lithographic reinforcement, and uniformity thereof, provided from neighboring diagonal conductor tracks.

An optimal layout density within the dynamic array is achieved by implementing the following design rules:

at least two metal **1** tracks be provided across the n-channel device area;

at least two metal **1** tracks be provided across the p-channel device area;

at least two gate electrode tracks be provided for the n-channel device; and

at least two gate electrode tracks be provided for the p-channel device.

Contacts and vias are becoming the most difficult mask from a lithographic point of view. This is because the contacts and vias are getting smaller, more closely spaced, and are randomly distributed. The spacing and density of the cuts (contact or vias) makes it extremely difficult to reliably print the shapes. For example, cut shapes may be printed improperly due to destructive interference patterns from neighboring shapes or lack of energy on lone shapes. If a cut is properly printed, the manufacturing yield of the associated contact or via is extremely high. Sub-resolution contacts can be provided to reinforce the exposure of the actual contacts, so long as the sub-resolution contacts do not resolve. Also, the sub-resolution contacts can be of any shape so long as they are smaller than the resolution capability of the lithographic process.

FIG. **13**A is an illustration showing an example of a sub-resolution contact layout used to lithographically reinforce diffusion contacts and gate electrode contacts, in accordance with one embodiment of the present invention. Sub-resolution contacts **1301** are drawn such that they are below the resolution of the lithographic system and will not be printed. The function of the sub-resolution contacts **1301** is to increase the light energy at the desired contact locations, e.g., **503**, **601**, through resonant imaging. In one embodiment, sub-resolution contacts **1301** are placed on a grid such that both gate electrode contacts **601** and diffusion contacts **503** are lithographically reinforced. For example, sub-resolution contacts **1301** are placed on a grid that is equal to one-half the diffusion contact **503** grid spacing to positively impact both gate electrode contacts **601** and diffusion contacts **503**. In one embodiment, a vertical spacing of the sub-resolution contacts **1301** follows the vertical spacing of the gate electrode contacts **601** and diffusion contacts **503**.

Grid location **1303** in FIG. **13**A denotes a location between adjacent gate electrode contacts **601**. Depending upon the lithographic parameters in the manufacturing process, it is possible that a sub-resolution contact **1301** at this grid location would create an undesirable bridge between the two adjacent gate electrode contacts **601**. If bridging is likely to occur, a sub-resolution contact **1301** at location **1303** can be omitted. Although FIG. **13**A shows an embodiment where sub-resolution contacts are placed adjacent to actual features to be resolved and not elsewhere, it should be understood that another embodiment may place a sub-resolution contact at each available grid location so as to fill the grid.

FIG. **13**B is an illustration showing the sub-resolution contact layout of FIG. **13**A with sub-resolution contacts defined to fill the grid to the extent possible, in accordance with one embodiment of the present invention. It should be appreciated that while the embodiment of FIG. **13**B fills the grid to the extent possible with sub-resolution contacts, placement of sub-resolution contacts is avoided at locations that would potentially cause undesirable bridging between adjacent fully resolved features.

FIG. **13**C is an illustration showing an example of a sub-resolution contact layout utilizing various shaped sub-resolution contacts, in accordance with one embodiment of the present invention. Alternative sub-resolution contact shapes can be utilized so long as the sub-resolution contacts are below the resolution capability of the manufacturing process. FIG. **13**C shows the use of "X-shaped" sub-resolution contacts **1305** to focus light energy at the corners of the adjacent contacts. In one embodiment, the ends of the X-shaped sub-resolution contact **1305** are extended to further enhance the deposition of light energy at the corners of the adjacent contacts.

FIG. **13**D is an illustration showing an exemplary implementation of alternate phase shift masking (APSM) with sub-resolution contacts, in accordance with one embodiment of the present invention. As in FIG. **13**A, sub-resolution contacts are utilized to lithographically reinforce diffusion contacts **503** and gate electrode contacts **601**. APSM is used to improve resolution when neighboring shapes create destructive interference patterns. The APSM technique modifies the mask so that the phase of light traveling through the mask on neighboring shapes is 180 degrees out of phase. This phase shift serves to remove destructive interference and allowing for greater contact density. By way of example, contacts in FIG. **13**D marked with a plus "+" sign represent contacts exposed with light waves of a first phase while contacts marked with a minus sign "−" represent contacts exposed with light waves that are shifted in phase by 180 degrees relative to the first phase used for the "+" sign contacts. It

should be appreciated that the APSM technique is utilized to ensure that adjacent contacts are separated from each other.

As feature sizes decrease, semiconductor dies are capable of including more gates. As more gates are included, however, the density of the interconnect layers begins to dictate the die size. This increasing demand on the interconnect layers drives higher levels of interconnect layers. However, the stacking of interconnect layers is limited in part by the topology of the underlying layers. For example, as interconnect layers are built up, islands, ridges, and troughs can occur. These islands, ridges, and troughs can cause breaks in the interconnect lines that cross them.

To mitigate these islands and troughs, the semiconductor manufacturing process utilizes a chemical mechanical polishing (CMP) procedure to mechanically and chemically polish the surface of the semiconductor wafer such that each subsequent interconnect layer is deposited on a substantially flat surface. Like the photolithography process the quality of the CMP process is layout pattern dependent. Specifically, an uneven distribution of a layout features across a die or a wafer can cause too much material to be removed in some places and not enough material to be removed in other places, thus causing variations in the interconnect thickness and unacceptable variations in the capacitance and resistance of the interconnect layer. The capacitance and resistance variation within the interconnect layer may alter the timing of a critical net causing design failure.

The CMP process requires that dummy fill be added in the areas without interconnect shapes so that a substantially uniform wafer topology is provided to avoid dishing and improve center-to-edge uniformity. Traditionally, dummy fill is placed post-design. Thus, in the traditional approach the designer is not aware of the dummy fill characteristics. Consequently, the dummy fill placed post-design may adversely influence the design performance in a manner that has not been evaluated by the designer. Also, because the conventional topology prior to the dummy fill is unconstrained, i.e., non-uniform, the post-design dummy fill will not be uniform and predictable. Therefore, in the conventional process, the capacitive coupling between the dummy fill regions and the neighboring active nets cannot be predicted by the designer.

As previously discussed, the dynamic array disclosed herein provides optimal regularity by maximally filling all interconnect tracks from gate electrode layer upward. If multiple nets are required in a single interconnect track, the interconnect track is split with a minimally spaced gap. For example, track **809** representing the metal **1** conduction line in FIG. **8**A represents three separate nets in the same track, where each net corresponds to a particular track segment. More specifically, there are two poly contact nets and a floating net to fill the track with minimal spacing between the track segments. The substantially complete filling of tracks maintains the regular pattern that creates resonant images across the dynamic array. Also, the regular architecture of the dynamic array with maximally filled interconnect tracks ensures that the dummy fill is placed in a uniform manner across the die. Therefore, the regular architecture of the dynamic array assists the CMP process to produce substantially uniform results across the die/wafer. Also, the regular gate pattern of the dynamic array assists with gate etching uniformity (microloading). Additionally, the regular architecture of the dynamic array combined with the maximally filled interconnect tracks allows the designer to analyze the capacitive coupling effects associated with the maximally filled tracks during the design phase and prior to fabrication.

Because the dynamic array sets the size and spacing of the linearly shaped features, i.e., tracks and contacts, in each mask layer, the design of the dynamic array can be optimized for the maximum capability of the manufacturing equipment and processes. That is to say, because the dynamic array is restricted to the regular architecture for each layer above diffusion, the manufacturer is capable of optimizing the manufacturing process for the specific characteristics of the regular architecture. It should be appreciated that with the dynamic array, the manufacturer does not have to be concerned with accommodating the manufacture of a widely varying set of arbitrarily-shaped layout features as is present in conventional unconstrained layouts.

An example of how the capability of manufacturing equipment can be optimized is provided as follows. Consider that a 90 nm process has a metal **2** pitch of 280 nm. This metal **2** pitch of 280 nm is not set by the maximum capability of equipment. Rather, this metal **2** pitch of 280 nm is set by the lithography of the vias. With the via lithography issues removed, the maximum capability of the equipment allows for a metal **2** pitch of about 220 nm Thus, the design rules for metal **2** pitch include about 25% margin to account for the light interaction unpredictability in the via lithography.

The regular architecture implemented within the dynamic array allows the light interaction unpredictability in the via lithography to be removed, thus allowing for a reduction in the metal **2** pitch margin. Such a reduction in the metal **2** pitch margin allows for a more dense design, i.e., allows for optimization of chip area utilization. Additionally, with the restricted, i.e., regular, topology afforded by the dynamic array, the margin in the design rules can be reduced. Moreover, not only can the excess margin beyond the capability of the process be reduced, the restricted topology afforded by the dynamic array also allows the number of required design rules to be substantially reduced. For example, a typical design rule set for an unconstrained topology could have more than 600 design rules. A design rule set for use with the dynamic array may have about 45 design rules. Therefore, the effort required to analyze and verify the design against the design rules is decreased by more than a factor of ten with the restricted topology of the dynamic array.

When dealing with line end-to-line end gaps (i.e., track segment-to-track segment gaps) in a given track of a mask layer in the dynamic array, a limited number of light interactions exist. This limited number of light interactions can be identified, predicted, and accurately compensated for ahead of time, dramatically reducing or completely eliminating the requirement for OPC/RET. The compensation for light interactions at line end-to-line end gaps represents a lithographic modification of the as-drawn feature, as opposed to a correction based on modeling of interactions, e.g., OPC/RET, associated with the as-drawn feature.

Also, with the dynamic array, changes to the as-drawn layout are only made where needed. In contrast, OPC is performed over an entire layout in a conventional design flow. In one embodiment, a correction model can be implemented as part of the layout generation for the dynamic array. For example, due to the limited number of possible line end gap interactions, a router can be programmed to insert a line break having characteristics defined as a function of its surroundings, i.e., as a function of its particular line end gap light interactions. It should be further appreciated that the regular architecture of the dynamic array allows the line ends to be adjusted by changing vertices rather than by adding vertices. Thus, in contrast with unconstrained topologies that rely on the OPC process, the dynamic array significantly reduces the cost and risk of mask production. Also, because the line end gap interactions in the dynamic array can be accurately predicted in the design phase, compensation for the predicted

line end gap interactions during the design phase does not increase risk of design failure.

In conventional unconstrained topologies, designers are required to have knowledge of the physics associated with the manufacturing process due to the presence of design dependent failures. With the grid-based system of the dynamic array as disclosed herein, the logical design can be separated from the physical design. More specifically, with the regular architecture of the dynamic array, the limited number of light interactions to be evaluated within the dynamic array, and the design independent nature of the dynamic array, designs can be represented using a grid point based netlist, as opposed to a physical netlist.

With the dynamic array, the design is not required to be represented in terms of physical information. Rather, the design can be represented as a symbolic layout. Thus, the designer can represent the design from a pure logic perspective without having to represent physical characteristics, e.g., sizes, of the design. It should be understood that the grid-based netlist, when translated to physical, matches the optimum design rules exactly for the dynamic array platform. When the grid-based dynamic array moves to a new technology, e.g., smaller technology, a grid-based netlist can be moved directly to the new technology because there is no physical data in the design representation. In one embodiment, the grid-based dynamic array system includes a rules database, a grid-based (symbolic) netlist, and the dynamic array architecture.

It should be appreciated that the grid-based dynamic array eliminates topology related failures associated with conventional unconstrained architectures. Also, because the manufacturability of the grid-based dynamic array is design independent, the yield of the design implemented on the dynamic array is independent of the design. Therefore, because the validity and yield of the dynamic array is preverified, the grid-based netlist can be implemented on the dynamic array with preverified yield performance.

FIG. **14** is an illustration showing a semiconductor chip structure **1400**, in accordance with one embodiment of the present invention. The semiconductor chip structure **1400** represents an exemplary portion of a semiconductor chip, including a diffusion region **1401** having a number of conductive lines **1403**A-**1403**G defined thereover. The diffusion region **1401** is defined in a substrate **1405**, to define an active region for at least one transistor device. The diffusion region **1401** can be defined to cover an area of arbitrary shape relative to the substrate **1405** surface.

The conductive lines **1403**A-**1403**G are arranged to extend over the substrate **1405** in a common direction **1407**. It should also be appreciated that each of the number of conductive lines **1403**A-**1403**G are restricted to extending over the diffusion region **1401** in the common direction **1407**. In one embodiment, the conductive lines **1403**A-**1403**G defined immediately over the substrate **1405** are polysilicon lines. In one embodiment, each of the conductive lines **1403**A-**1403**G is defined to have essentially the same width **1409** in a direction perpendicular to the common direction **1407** of extension. In another embodiment, some of the conductive lines **1403**A-**1403**G are defined to have different widths relative to the other conductive lines. However, regardless of the width of the conductive lines **1403**A-**1403**G, each of the conductive lines **1403**A-**1403**G is spaced apart from adjacent conductive lines according to essentially the same center-to-center pitch **1411**.

As shown in FIG. **14**, some of the conductive lines (**1403**B-**1403**E) extend over the diffusion region **1401**, and other conductive lines (**1403**A, **1403**F, **1403**G) extend over non-diffusion portions the substrate **1405**. It should be appreciated that the conductive lines **1403**A-**1403**G maintain their width **1409** and pitch **1411** regardless of whether they are defined over diffusion region **1401** or not. Also, it should be appreciated that the conductive lines **1403**A-**1403**G maintain essentially the same length **1413** regardless of whether they are defined over diffusion region **1401** or not, thereby maximizing lithographic reinforcement between the conductive lines **1403**A-**1403**G across the substrate. In this manner, some of the conductive lines, e.g., **1403**D, defined over the diffusion region **1401** include a necessary active portion **1415**, and one or more uniformity extending portions **1417**.

It should be appreciated that the semiconductor chip structure **1400** represents a portion of the dynamic array described above with respect to FIGS. **2**-**13**D. Therefore, it should be understood that the uniformity extending portions **1417** of the conductive lines (**1403**B-**1403**E) are present to provide lithographic reinforcement of neighboring conductive lines **1403**A-**1403**G. Also, although they may not be required for circuit operation, each of conductive lines **1403**A, **1403**F, and **1403**G are present to provide lithographic reinforcement of neighboring conductive lines **1403**A-**1403**G.

The concept of the necessary active portion **1415** and the uniformity extending portions **1417** also applies to higher level interconnect layers. As previously described with regard to the dynamic array architecture, adjacent interconnect layers traverse over the substrate in transverse directions, e.g., perpendicular or diagonal directions, to enable routing/connectivity required by the logic device implemented within the dynamic array. As with the conductive lines **1403**A-**1403**G, each of the conductive lines within an interconnect layer may include a required portion (necessary active portion) to enable required routing/connectivity, and a non-required portion (uniformity extending portion) to provide lithographic reinforcement to neighboring conductive lines. Also, as with the conductive lines **1403**A-**1403**G, the conductive lines within an interconnect layer extend in a common direction over the substrate, have essentially the same width, and are spaced apart from each other according to an essentially constant pitch.

In one embodiment, conductive lines within an interconnect layer follow essentially the same ratio between line width and line spacing. For example, at 90 nm the metal **4** pitch is 280 nm with a line width and line spacing equal to 140 nm. Larger conductive lines can be printed on a larger line pitch if the line width is equal to the line spacing.

FIG. **14**A shows an annotated version of FIG. **14**. The features depicted in FIG. **14**A are exactly the same as the features depicted in FIG. **14**. FIG. **14**A shows each of the conductive lines **1403**B and **1403**C to have a uniformity extending portion **14***a***01** as measured in the common direction **1407**. FIG. **14**A shows each of the conductive lines **1403**D and **1403**E to have a uniformity extending portion **14***a***03** as measured in the common direction **1407**. FIG. **14**A shows each of the conductive lines **1403**B, **1403**C, **1403**D, and **1403**E to have a uniformity extending portion **14***a***05** as measured in the common direction **1407**. FIG. **15** shows an example layout architecture defined in accordance with one embodiment of the present invention. The layout architecture follows a grid pattern and is based upon a horizontal grid and a vertical grid. The horizontal grid is set by the poly gate pitch. The vertical pitch is set by the metal **1**/metal **3** pitch. All of the rectangular shapes should be centered on a grid point. The layout architecture minimizes the use of bends to eliminate unpredictable lithographic interactions. Bends are allowed on

the diffusion layer to control transistor device sizes. Other layers should be rectangular in shape and fixed in one dimension.

FIG. **15**A shows an annotated version of FIG. **15**. The features depicted in FIG. **15**A are exactly the same as the features depicted in FIG. **15**. FIG. **15**A shows a first electrical connection **15***a***01** (as denoted by the heavy solid black line). FIG. **15**A shows a second electrical connection **15***a***03** (as denoted by the heavy dashed black line).

The invention described herein can be embodied as computer readable code on a computer readable medium. The computer readable medium is any data storage device that can store data which can be thereafter be read by a computer system. Examples of the computer readable medium include hard drives, network attached storage (NAS), read-only memory, random-access memory, CD-ROMs, CD-Rs, CD-RWs, magnetic tapes, and other optical and non-optical data storage devices. The computer readable medium can also be distributed over a network coupled computer systems so that the computer readable code is stored and executed in a distributed fashion. Additionally, a graphical user interface (GUI) implemented as computer readable code on a computer readable medium can be developed to provide a user interface for performing any embodiment of the present invention.

While this invention has been described in terms of several embodiments, it will be appreciated that those skilled in the art upon reading the preceding specifications and studying the drawings will realize various alterations, additions, permutations and equivalents thereof. Therefore, it is intended that the present invention includes all such alterations, additions, permutations, and equivalents as fall within the true spirit and scope of the invention.

What is claimed is:

**1**. A semiconductor chip, comprising:

a region including a plurality of transistors, each of the plurality of transistors in the region forming part of circuitry associated with execution of one or more logic functions, the region including at least eight conductive structures formed within the semiconductor chip, some of the at least eight conductive structures forming at least one transistor gate electrode,

each of the at least eight conductive structures respectively having a corresponding top surface, wherein an entirety of a periphery of the corresponding top surface is defined by a corresponding first end, a corresponding second end, a corresponding first edge, and a corresponding second edge, such that a total distance along the entirety of the periphery of the corresponding top surface is equal to a sum of a total distance along the corresponding first edge and a total distance along the corresponding second edge and a total distance along the corresponding first end and a total distance along the corresponding second end,

wherein the total distance along the corresponding first edge is greater than two times the total distance along the corresponding first end,

wherein the total distance along the corresponding first edge is greater than two times the total distance along the corresponding second end,

wherein the total distance along the corresponding second edge is greater than two times the total distance along the corresponding first end,

wherein the total distance along the corresponding second edge is greater than two times the total distance along the corresponding second end,

wherein the corresponding first end extends from the corresponding first edge to the corresponding second edge and is located principally within a space between the corresponding first and second edges,

wherein the corresponding second end extends from the corresponding first edge to the corresponding second edge and is located principally within the space between the corresponding first and second edges,

the top surfaces of the at least eight conductive structures co-planar with each other,

each of the at least eight conductive structures having a corresponding lengthwise centerline oriented in a first direction along its top surface and extending from its first end to its second end,

each of the at least eight conductive structures having a length as measured along its lengthwise centerline from its first end to its second end,

wherein the first edge of each of the at least eight conductive structures is substantially straight,

wherein the second edge of each of the at least eight conductive structures is substantially straight,

each of the at least eight conductive structures having both its first edge and its second edge oriented substantially parallel to its lengthwise centerline,

each of the at least eight conductive structures having a width measured in a second direction perpendicular to the first direction at a midpoint of its lengthwise centerline,

each of the first direction and the second direction oriented substantially parallel to the co-planar top surfaces of the at least eight conductive structures,

wherein the at least eight conductive structures are positioned in a side-by-side manner such that each of the at least eight conductive structures is positioned to have at least a portion of its length beside at least a portion of the length of another of the at least eight conductive structures,

wherein the width of each of the at least eight conductive structures is less than 45 nanometers, the region having a size of about 965 nanometers as measured in the second direction, each of the at least eight conductive structures positioned such that a distance as measured in the second direction between its lengthwise centerline and the lengthwise centerline of at least one other of the at least eight conductive structures is substantially equal to a first pitch that is less than or equal to about 193 nanometers,

wherein the at least eight conductive structures includes a first conductive structure, the first conductive structure including a portion that forms a gate electrode of first transistor of a first transistor type, the first conductive structure including a portion that forms a gate electrode of a first transistor of a second transistor type,

wherein the at least eight conductive structures includes a second conductive structure, the second conductive structure including a portion that forms a gate electrode of a second transistor of the first transistor type, wherein any transistor having its gate electrode formed by the second conductive structure is of the first transistor type,

wherein the at least eight conductive structures includes a third conductive structure, the third conductive structure including a portion that forms a gate electrode of a second transistor of the second transistor type, wherein any transistor having its gate electrode formed by the third conductive structure is of the second transistor type,

wherein the at least eight conductive structures includes a fourth conductive structure, the fourth conductive structure including a portion that forms a gate electrode of a

third transistor of the first transistor type, wherein any transistor having its gate electrode formed by the fourth conductive structure is of the first transistor type,

wherein the at least eight conductive structures includes a fifth conductive structure, the fifth conductive structure including a portion that forms a gate electrode of a third transistor of the second transistor type, wherein any transistor having its gate electrode formed by the fifth conductive structure is of the second transistor type,

wherein the first transistor of the first transistor type includes a first diffusion terminal and the second transistor of the first transistor type includes a first diffusion terminal, the first diffusion terminal of the first transistor of the first transistor type electrically connected to the first diffusion terminal of the second transistor of the first transistor type through a first electrical connection,

wherein the first transistor of the second transistor type includes a first diffusion terminal, and the second transistor of the second transistor type includes a first diffusion terminal, the first diffusion terminal of the first transistor of the second transistor type electrically connected to the first diffusion terminal of the second transistor of the second transistor type through a second electrical connection,

wherein the second transistor of the first transistor type includes a second diffusion terminal, and the third transistor of the first transistor type includes a first diffusion terminal, the second diffusion terminal of the second transistor of the first transistor type electrically connected to the first diffusion terminal of the third transistor of the first transistor type through a third electrical connection,

wherein the second transistor of the second transistor type includes a second diffusion terminal, and the third transistor of the second transistor type includes a first diffusion terminal, the second diffusion terminal of the second transistor of the second transistor type electrically connected to the first diffusion terminal of the third transistor of the second transistor type through a fourth electrical connection,

wherein the third transistor of the first transistor type includes a second diffusion terminal electrically connected to a first diffusion terminal of a fourth transistor of the first transistor type through a fifth electrical connection,

wherein the third transistor of the second transistor type includes a second diffusion terminal electrically connected to a first diffusion terminal of a fourth transistor of the second transistor type through a sixth electrical connection,

wherein the third electrical connection is electrically connected to the fourth electrical connection through a seventh electrical connection,

wherein the gate electrode of the second transistor of the first transistor type is electrically connected to the gate electrode of the third transistor of the second transistor type through an eighth electrical connection,

wherein the gate electrode of the third transistor of the first transistor type is electrically connected to the gate electrode of the second transistor of the second transistor type through a ninth electrical connection,

wherein each transistor of the first transistor type having its gate electrode formed by any of the at least eight conductive structures is included in a first collection of transistors, and wherein each transistor of the second transistor type having its gate electrode formed by any of the at least eight conductive structures is included in a second collection of transistors, wherein the first collection of transistors is separated from the second collection of transistors by an inner sub-region of the region, wherein the inner sub-region does not include a source or a drain of any transistor.

**2**. The semiconductor chip as recited in claim **1**, wherein the region includes a first interconnect conductive structure positioned within either of a first interconnect level, a second interconnect level, a third interconnect level, or a fourth interconnect level,

the first interconnect conductive structure having a top surface, an entirety of a periphery of the top surface of the first interconnect conductive structure defined by a first end of the first interconnect conductive structure, a second end of the first interconnect conductive structure, a first edge of the first interconnect conductive structure, and a second edge of the first interconnect conductive structure, such that a total distance along the entirety of the periphery of the top surface of the first interconnect conductive structure is equal to a sum of a total distance along the first edge of the first interconnect conductive structure and a total distance along the second edge of the first interconnect conductive structure and a total distance along the first end of the first interconnect conductive structure and a total distance along the second end of the first interconnect conductive structure,

wherein the total distance along the first edge of the first interconnect conductive structure is greater than two times the total distance along the first end of the first interconnect conductive structure,

wherein the total distance along the first edge of the first interconnect conductive structure is greater than two times the total distance along the second end of the first interconnect conductive structure,

wherein the total distance along the second edge of the first interconnect conductive structure is greater than two times the total distance along the first end of the first interconnect conductive structure,

wherein the total distance along the second edge of the first interconnect conductive structure is greater than two times the total distance along the second end of the first interconnect conductive structure,

wherein the first end of the first interconnect conductive structure extends from the first edge of the first interconnect conductive structure to the second edge of the first interconnect conductive structure and is located principally within a space between the first and second edges of the first interconnect conductive structure,

wherein the second end of the first interconnect conductive structure extends from the first edge of the first interconnect conductive structure to the second edge of the first interconnect conductive structure and is located principally within the space between the first and second edges of the first interconnect conductive structure,

the first interconnect conductive structure having a lengthwise centerline oriented in the first direction along its top surface and extending from its first end to its second end,

wherein the first edge of the first interconnect conductive structure is substantially straight and is oriented substantially parallel to the lengthwise centerline of the first interconnect conductive structure,

wherein the second edge of the first interconnect conductive structure is substantially straight and is oriented substantially parallel to the lengthwise centerline of the first interconnect conductive structure,

wherein the first interconnect conductive structure has a length measured along its lengthwise centerline from its first end to its second end,

wherein the first interconnect conductive structure has a width measured in the second direction perpendicular to the first direction at a midpoint of the lengthwise centerline of the first interconnect conductive structure,

wherein the first interconnect level is formed at a vertical position within the semiconductor chip above the at least eight conductive structures, wherein the first interconnect level is separated from the co-planar top surfaces of the at least eight conductive structures by at least one dielectric material,

wherein the second interconnect level is formed at a vertical position within the semiconductor chip above the first interconnect level,

wherein the third interconnect level is formed at a vertical position within the semiconductor chip above the second interconnect level, and

wherein the fourth interconnect level is formed at a vertical position within the semiconductor chip above the third interconnect level.

**3**. The semiconductor chip as recited in claim **2**, wherein the region includes a second interconnect conductive structure positioned next to and spaced apart from the first interconnect conductive structure in a same interconnect level as the first interconnect conductive structure,

the second interconnect conductive structure having a top surface, an entirety of a periphery of the top surface of the second interconnect conductive structure defined by a first end of the second interconnect conductive structure, a second end of the second interconnect conductive structure, a first edge of the second interconnect conductive structure, and a second edge of the second interconnect conductive structure, such that a total distance along the entirety of the periphery of the top surface of the second interconnect conductive structure is equal to a sum of a total distance along the first edge of the second interconnect conductive structure and a total distance along the second edge of the second interconnect conductive structure and a total distance along the first end of the second interconnect conductive structure and a total distance along the second end of the second interconnect conductive structure,

wherein the total distance along the first edge of the second interconnect conductive structure is greater than two times the total distance along the first end of the second interconnect conductive structure,

wherein the total distance along the first edge of the second interconnect conductive structure is greater than two times the total distance along the second end of the second interconnect conductive structure,

wherein the total distance along the second edge of the second interconnect conductive structure is greater than two times the total distance along the first end of the second interconnect conductive structure,

wherein the total distance along the second edge of the second interconnect conductive structure is greater than two times the total distance along the second end of the second interconnect conductive structure,

wherein the first end of the second interconnect conductive structure extends from the first edge of the second interconnect conductive structure to the second edge of the second interconnect conductive structure and is located principally within a space between the first and second edges of the second interconnect conductive structure,

wherein the second end of the second interconnect conductive structure extends from the first edge of the second interconnect conductive structure to the second edge of the second interconnect conductive structure and is located principally within the space between the first and second edges of the second interconnect conductive structure,

the second interconnect conductive structure having a lengthwise centerline oriented in the first direction along its top surface and extending from its first end to its second end,

wherein the first edge of the second interconnect conductive structure is substantially straight and is oriented substantially parallel to the lengthwise centerline of the second interconnect conductive structure,

wherein the second edge of the second interconnect conductive structure is substantially straight and is oriented substantially parallel to the lengthwise centerline of the second interconnect conductive structure,

wherein the second interconnect conductive structure has a length measured along its lengthwise centerline from its first end to its second end,

wherein the second interconnect conductive structure has a width measured in the second direction perpendicular to the first direction at a midpoint of the lengthwise centerline of the second interconnect conductive structure.

**4**. The semiconductor chip as recited in claim **3**, wherein the first and second interconnect conductive structures are positioned such that a distance as measured in the second direction between their lengthwise centerlines is substantially equal to a second pitch, wherein the second pitch is a fractional multiple of the first pitch.

**5**. The semiconductor chip as recited in claim **4**, wherein the second pitch is less than or equal to the first pitch.

**6**. The semiconductor chip as recited in claim **5**, wherein at least one of the at least eight conductive structures within the region does not form a gate electrode of any transistor and has a width as measured in the second direction that is substantially equal to a width as measured in the second direction of another of the at least eight conductive structures.

**7**. The semiconductor chip as recited in claim **6**, wherein the first and second interconnect conductive structures are positioned within either of the first interconnect level, the second interconnect level, or the third interconnect level.

**8**. The semiconductor chip as recited in claim **1**, wherein the region includes a first interconnect conductive structure positioned within either of a first interconnect level, a second interconnect level, a third interconnect level, or a fourth interconnect level,

the first interconnect conductive structure having a top surface, an entirety of a periphery of the top surface of the first interconnect conductive structure defined by a first end of the first interconnect conductive structure, a second end of the first interconnect conductive structure, a first edge of the first interconnect conductive structure, and a second edge of the first interconnect conductive structure, such that a total distance along the entirety of the periphery of the top surface of the first interconnect conductive structure is equal to a sum of a total distance along the first edge of the first interconnect conductive structure and a total distance along the second edge of the first interconnect conductive structure and a total distance along the first end of the first interconnect conductive structure and a total distance along the second end of the first interconnect conductive structure,

wherein the total distance along the first edge of the first interconnect conductive structure is greater than two

times the total distance along the first end of the first interconnect conductive structure,

wherein the total distance along the first edge of the first interconnect conductive structure is greater than two times the total distance along the second end of the first interconnect conductive structure,

wherein the total distance along the second edge of the first interconnect conductive structure is greater than two times the total distance along the first end of the first interconnect conductive structure,

wherein the total distance along the second edge of the first interconnect conductive structure is greater than two times the total distance along the second end of the first interconnect conductive structure,

wherein the first end of the first interconnect conductive structure extends from the first edge of the first interconnect conductive structure to the second edge of the first interconnect conductive structure and is located principally within a space between the first and second edges of the first interconnect conductive structure,

wherein the second end of the first interconnect conductive structure extends from the first edge of the first interconnect conductive structure to the second edge of the first interconnect conductive structure and is located principally within the space between the first and second edges of the first interconnect conductive structure,

the first interconnect conductive structure having a lengthwise centerline oriented in the second direction along its top surface and extending from its first end to its second end,

wherein the first edge of the first interconnect conductive structure is substantially straight and is oriented substantially parallel to the lengthwise centerline of the first interconnect conductive structure,

wherein the second edge of the first interconnect conductive structure is substantially straight and is oriented substantially parallel to the lengthwise centerline of the first interconnect conductive structure,

wherein the first interconnect conductive structure has a length measured along its lengthwise centerline from its first end to its second end,

wherein the first interconnect conductive structure has a width measured in the first direction perpendicular to the second direction at a midpoint of the lengthwise centerline of the first interconnect conductive structure,

wherein the first interconnect level is formed at a vertical position within the semiconductor chip above the at least eight conductive structures, wherein the first interconnect level is separated from the co-planar top surfaces of the at least eight conductive structures by at least one dielectric material,

wherein the second interconnect level is formed at a vertical position within the semiconductor chip above the first interconnect level,

wherein the third interconnect level is formed at a vertical position within the semiconductor chip above the second interconnect level, and

wherein the fourth interconnect level is formed at a vertical position within the semiconductor chip above the third interconnect level.

**9**. The semiconductor chip as recited in claim **8**, wherein the region includes a second interconnect conductive structure positioned in a same interconnect level as the first interconnect conductive structure,

the second interconnect conductive structure having a top surface, an entirety of a periphery of the top surface of the second interconnect conductive structure defined by a first end of the second interconnect conductive structure, a second end of the second interconnect conductive structure, a first edge of the second interconnect conductive structure, and a second edge of the second interconnect conductive structure, such that a total distance along the entirety of the periphery of the top surface of the second interconnect conductive structure is equal to a sum of a total distance along the first edge of the second interconnect conductive structure and a total distance along the second edge of the second interconnect conductive structure and a total distance along the first end of the second interconnect conductive structure and a total distance along the second end of the second interconnect conductive structure,

wherein the total distance along the first edge of the second interconnect conductive structure is greater than two times the total distance along the first end of the second interconnect conductive structure,

wherein the total distance along the first edge of the second interconnect conductive structure is greater than two times the total distance along the second end of the second interconnect conductive structure,

wherein the total distance along the second edge of the second interconnect conductive structure is greater than two times the total distance along the first end of the second interconnect conductive structure,

wherein the total distance along the second edge of the second interconnect conductive structure is greater than two times the total distance along the second end of the second interconnect conductive structure,

wherein the first end of the second interconnect conductive structure extends from the first edge of the second interconnect conductive structure to the second edge of the second interconnect conductive structure and is located principally within a space between the first and second edges of the second interconnect conductive structure,

wherein the second end of the second interconnect conductive structure extends from the first edge of the second interconnect conductive structure to the second edge of the second interconnect conductive structure and is located principally within the space between the first and second edges of the second interconnect conductive structure,

the second interconnect conductive structure having a lengthwise centerline oriented in the second direction along its top surface and extending from its first end to its second end,

wherein the first edge of the second interconnect conductive structure is substantially straight and is oriented substantially parallel to the lengthwise centerline of the second interconnect conductive structure,

wherein the second edge of the second interconnect conductive structure is substantially straight and is oriented substantially parallel to the lengthwise centerline of the second interconnect conductive structure,

wherein the second interconnect conductive structure has a length measured along its lengthwise centerline from its first end to its second end,

wherein the second interconnect conductive structure has a width measured in the first direction perpendicular to the second direction at a midpoint of the lengthwise centerline of the second interconnect conductive structure,

wherein the first and second interconnect conductive structures are positioned next to and spaced apart from each other such that a distance as measured in the first direction between their lengthwise centerlines is substantially equal to a second pitch.

10. The semiconductor chip as recited in claim 9, wherein the region includes a third interconnect conductive structure positioned in the same interconnect level as the first and second interconnect conductive structures,

the third interconnect conductive structure having a top surface, an entirety of a periphery of the top surface of the third interconnect conductive structure defined by a first end of the third interconnect conductive structure, a second end of the third interconnect conductive structure, a first edge of the third interconnect conductive structure, and a second edge of the third interconnect conductive structure, such that a total distance along the entirety of the periphery of the top surface of the third interconnect conductive structure is equal to a sum of a total distance along the first edge of the third interconnect conductive structure and a total distance along the second edge of the third interconnect conductive structure and a total distance along the first end of the third interconnect conductive structure and a total distance along the second end of the third interconnect conductive structure,

wherein the total distance along the first edge of the third interconnect conductive structure is greater than two times the total distance along the first end of the third interconnect conductive structure,

wherein the total distance along the first edge of the third interconnect conductive structure is greater than two times the total distance along the second end of the third interconnect conductive structure,

wherein the total distance along the second edge of the third interconnect conductive structure is greater than two times the total distance along the first end of the third interconnect conductive structure,

wherein the total distance along the second edge of the third interconnect conductive structure is greater than two times the total distance along the second end of the third interconnect conductive structure,

wherein the first end of the third interconnect conductive structure extends from the first edge of the third interconnect conductive structure to the second edge of the third interconnect conductive structure and is located principally within a space between the first and second edges of the third interconnect conductive structure,

wherein the second end of the third interconnect conductive structure extends from the first edge of the third interconnect conductive structure to the second edge of the third interconnect conductive structure and is located principally within the space between the first and second edges of the third interconnect conductive structure,

the third interconnect conductive structure having a lengthwise centerline oriented in the second direction along its top surface and extending from its first end to its second end,

wherein the first edge of the third interconnect conductive structure is substantially straight and is oriented substantially parallel to the lengthwise centerline of the third interconnect conductive structure,

wherein the second edge of the third interconnect conductive structure is substantially straight and is oriented substantially parallel to the lengthwise centerline of the third interconnect conductive structure,

wherein the third interconnect conductive structure has a length measured along its lengthwise centerline from its first end to its second end,

wherein the third interconnect conductive structure has a width measured in the first direction perpendicular to the second direction at a midpoint of the lengthwise centerline of the third interconnect conductive structure,

wherein the region includes a fourth interconnect conductive structure positioned in the same interconnect level as the first, second, and third interconnect conductive structures,

the fourth interconnect conductive structure having a top surface, an entirety of a periphery of the top surface of the fourth interconnect conductive structure defined by a first end of the fourth interconnect conductive structure, a second end of the fourth interconnect conductive structure, a first edge of the fourth interconnect conductive structure, and a second edge of the fourth interconnect conductive structure, such that a total distance along the entirety of the periphery of the top surface of the fourth interconnect conductive structure is equal to a sum of a total distance along the first edge of the fourth interconnect conductive structure and a total distance along the second edge of the fourth interconnect conductive structure and a total distance along the first end of the fourth interconnect conductive structure and a total distance along the second end of the fourth interconnect conductive structure,

wherein the total distance along the first edge of the fourth interconnect conductive structure is greater than two times the total distance along the first end of the fourth interconnect conductive structure,

wherein the total distance along the first edge of the fourth interconnect conductive structure is greater than two times the total distance along the second end of the fourth interconnect conductive structure,

wherein the total distance along the second edge of the fourth interconnect conductive structure is greater than two times the total distance along the first end of the fourth interconnect conductive structure,

wherein the total distance along the second edge of the fourth interconnect conductive structure is greater than two times the total distance along the second end of the fourth interconnect conductive structure,

wherein the first end of the fourth interconnect conductive structure extends from the first edge of the fourth interconnect conductive structure to the second edge of the fourth interconnect conductive structure and is located principally within a space between the first and second edges of the fourth interconnect conductive structure,

wherein the second end of the fourth interconnect conductive structure extends from the first edge of the fourth interconnect conductive structure to the second edge of the fourth interconnect conductive structure and is located principally within the space between the first and second edges of the fourth interconnect conductive structure,

the fourth interconnect conductive structure having a lengthwise centerline oriented in the second direction along its top surface and extending from its first end to its second end,

wherein the first edge of the fourth interconnect conductive structure is substantially straight and is oriented substantially parallel to the lengthwise centerline of the fourth interconnect conductive structure,

wherein the second edge of the fourth interconnect conductive structure is substantially straight and is oriented substantially parallel to the lengthwise centerline of the fourth interconnect conductive structure,

wherein the fourth interconnect conductive structure has a length measured along its lengthwise centerline from its first end to its second end,

wherein the fourth interconnect conductive structure has a width measured in the first direction perpendicular to the second direction at a midpoint of the lengthwise centerline of the fourth interconnect conductive structure,

wherein the third and fourth interconnect conductive structures are positioned next to and spaced apart from each other such that a distance as measured in the first direction between their lengthwise centerlines is substantially equal to the second pitch.

**11**. The semiconductor chip as recited in claim **10**, wherein at least one of the at least eight conductive structures within the region does not form a gate electrode of any transistor and has a width as measured in the second direction that is substantially equal to a width as measured in the second direction of another of the at least eight conductive structures.

**12**. The semiconductor chip as recited in claim **11**, wherein the first, second, and third interconnect conductive structures are positioned within either of the first interconnect level, the second interconnect level, or the third interconnect level.

**13**. The semiconductor chip as recited in claim **1**, wherein the eighth electrical connection includes one or more overlying interconnect conductive structures, or the ninth electrical connection includes one or more overlying interconnect conductive structures, or both the eighth and the ninth electrical connections include one or more overlying electrical connections, wherein each overlying interconnect conductive structure is formed at a respective vertical position within the semiconductor chip overlying some of the at least eight conductive structures so as to be separated from the co-planar top surfaces of the at least eight conductive structures by at least one dielectric material,

wherein each overlying interconnect conductive structure that is part of the eighth or ninth electrical connection has a respective top surface with an entirety of a periphery of the respective top surface defined by a corresponding first end, a corresponding second end, a corresponding first edge, and a corresponding second edge, such that a total distance along the entirety of the periphery of the respective top surface is equal to a sum of a total distance along the corresponding first edge and a total distance along the corresponding second edge and a total distance along the corresponding first end and a total distance along the corresponding second end,

wherein the total distance along the corresponding first edge is greater than two times the total distance along the corresponding first end and is greater than two times the total distance along the corresponding second end, wherein the total distance along the corresponding second edge is greater than two times the total distance along the corresponding first end and is greater than two times the total distance along the corresponding second end,

wherein the corresponding first end extends from the corresponding first edge to the corresponding second edge and is located principally within a space between the corresponding first edge and the corresponding second edge, wherein the corresponding second end extends from the corresponding first edge to the corresponding second edge and is located principally within a space between the corresponding first edge and the corresponding second edge,

wherein each overlying interconnect conductive structure that is part of the eighth or ninth electrical connection has a respective lengthwise centerline oriented along its respective top surface to extend from its corresponding first end to its corresponding second end, with each of the corresponding first edge and the corresponding second edge being substantially straight and oriented substantially parallel to its respective lengthwise centerline.

**14**. The semiconductor chip as recited in claim **1**, wherein the lengthwise centerline of the second conductive structure is substantially aligned with the lengthwise centerline of the third conductive structure, and wherein the lengthwise centerline of the fourth conductive structure is substantially aligned with the lengthwise centerline of the fifth conductive structure.

**15**. The semiconductor chip as recited in claim **14**, wherein a gate electrode of the fourth transistor of the first transistor type and a gate electrode of the fourth transistor of the second transistor type are formed by respective portions of a single one of the at least eight conductive structures.

**16**. The semiconductor chip as recited in claim **15**, wherein at least one of the at least eight conductive structures within the region is a non-gate forming conductive structure that does not form a gate electrode of any transistor,

the non-gate forming conductive structure positioned between at least two neighboring conductive structures of the at least eight conductive structures, with at least one of the at least two neighboring conductive structures forming at least one gate electrode of at least one transistor,

the non-gate forming conductive structure positioned such that its lengthwise centerline is separated from the lengthwise centerlines of each of the at least two neighboring conductive structures by the first pitch as measured in the second direction,

the non-gate forming conductive structure having a width as measured in the second direction that is substantially equal to a width as measured in the second direction of at least one of the at least two neighboring conductive structures.

**17**. The semiconductor chip as recited in claim **16**, wherein the region includes a first connection forming conductive structure positioned to physically join to the top surface of the second conductive structure, wherein the first connection forming conductive structure is positioned a first connection distance away from a nearest gate electrode forming portion of the second conductive structure, the first connection distance measured in the first direction between closest located portions of the first connection forming conductive structure and the nearest gate electrode forming portion of the second conductive structure,

wherein the region includes a second connection forming conductive structure positioned to physically join to the top surface of the third conductive structure, wherein the second connection forming conductive structure is positioned a second connection distance away from a nearest gate electrode forming portion of the third conductive structure, the second connection distance measured in the first direction between closest located portions of the second connection forming conductive structure and the nearest gate electrode forming portion of the third conductive structure,

wherein the region includes a third connection forming conductive structure positioned to physically join to the top surface of the fourth conductive structure, wherein the third connection forming conductive structure is positioned a third connection distance away from a nearest gate electrode forming portion of the fourth conductive structure, the third connection distance measured in the first direction between closest located portions of the third connection forming conductive structure and the nearest gate electrode forming portion of the fourth conductive structure,

wherein the region includes a fourth connection forming conductive structure positioned to physically join to the top surface of the fifth conductive structure, wherein the fourth connection forming conductive structure is positioned a fourth connection distance away from a nearest gate electrode forming portion of the fifth conductive structure, the fourth connection distance measured in the first direction between closest located portions of the fourth connection forming conductive structure and the nearest gate electrode forming portion of the fifth conductive structure,

wherein at least two of the first, second, third, and fourth connection distances are different.

**18**. The semiconductor chip as recited in claim **17**, wherein the seventh electrical connection includes one or more overlying interconnect conductive structures formed at a respective vertical position within the semiconductor chip overlying some of the at least eight conductive structures so as to be separated from the co-planar top surfaces of the at least eight conductive structures by at least one dielectric material,

wherein each overlying interconnect conductive structure that is part of the seventh electrical connection has a respective top surface with an entirety of a periphery of the respective top surface defined by a corresponding first end, a corresponding second end, a corresponding first edge, and a corresponding second edge, such that a total distance along the entirety of the periphery of the respective top surface is equal to a sum of a total distance along the corresponding first edge and a total distance along the corresponding second edge and a total distance along the corresponding first end and a total distance along the corresponding second end,

wherein the total distance along the corresponding first edge is greater than two times the total distance along the corresponding first end and is greater than two times the total distance along the corresponding second end, wherein the total distance along the corresponding second edge is greater than two times the total distance along the corresponding first end and is greater than two times the total distance along the corresponding second end,

wherein the corresponding first end extends from the corresponding first edge to the corresponding second edge and is located principally within a space between the corresponding first edge and the corresponding second edge, wherein the corresponding second end extends from the corresponding first edge to the corresponding second edge and is located principally within a space between the corresponding first edge and the corresponding second edge,

wherein each overlying interconnect conductive structure that is part of the seventh electrical connection has a respective lengthwise centerline oriented along its respective top surface to extend from its corresponding first end to its corresponding second end, with each of the corresponding first edge and the corresponding second edge being substantially straight and oriented substantially parallel to its respective lengthwise centerline.

**19**. The semiconductor chip as recited in claim **18**, wherein the eighth electrical connection includes one or more overlying interconnect conductive structures formed at a respective vertical position within the semiconductor chip overlying some of the at least eight conductive structures so as to be separated from the co-planar top surfaces of the at least eight conductive structures by at least one dielectric material,

wherein each overlying interconnect conductive structure that is part of the eighth electrical connection has a respective top surface with an entirety of a periphery of the respective top surface defined by a corresponding first end, a corresponding second end, a corresponding first edge, and a corresponding second edge, such that a total distance along the entirety of the periphery of the respective top surface is equal to a sum of a total distance along the corresponding first edge and a total distance along the corresponding second edge and a total distance along the corresponding first end and a total distance along the corresponding second end,

wherein the total distance along the corresponding first edge is greater than two times the total distance along the corresponding first end and is greater than two times the total distance along the corresponding second end, wherein the total distance along the corresponding second edge is greater than two times the total distance along the corresponding first end and is greater than two times the total distance along the corresponding second end,

wherein the corresponding first end extends from the corresponding first edge to the corresponding second edge and is located principally within a space between the corresponding first edge and the corresponding second edge, wherein the corresponding second end extends from the corresponding first edge to the corresponding second edge and is located principally within a space between the corresponding first edge and the corresponding second edge,

wherein each overlying interconnect conductive structure that is part of the eighth electrical connection has a respective lengthwise centerline oriented along its respective top surface to extend from its corresponding first end to its corresponding second end, with each of the corresponding first edge and the corresponding second edge being substantially straight and oriented substantially parallel to its respective lengthwise centerline.

**20**. The semiconductor chip as recited in claim **14**, wherein the eighth electrical connection includes one or more overlying interconnect conductive structures formed at a respective vertical position within the semiconductor chip overlying some of the at least eight conductive structures so as to be separated from the co-planar top surfaces of the at least eight conductive structures by at least one dielectric material,

wherein each overlying interconnect conductive structure that is part of the eighth electrical connection has a respective top surface with an entirety of a periphery of the respective top surface defined by a corresponding first end, a corresponding second end, a corresponding first edge, and a corresponding second edge, such that a total distance along the entirety of the periphery of the respective top surface is equal to a sum of a total distance along the corresponding first edge and a total distance along the corresponding second edge and a total distance along the corresponding first end and a total distance along the corresponding second end,

wherein the total distance along the corresponding first edge is greater than two times the total distance along the corresponding first end and is greater than two times the total distance along the corresponding second end, wherein the total distance along the corresponding second edge is greater than two times the total distance along the corresponding first end and is greater than two times the total distance along the corresponding second end,

wherein the corresponding first end extends from the corresponding first edge to the corresponding second edge and is located principally within a space between the

corresponding first edge and the corresponding second edge, wherein the corresponding second end extends from the corresponding first edge to the corresponding second edge and is located principally within a space between the corresponding first edge and the corresponding second edge,

wherein each overlying interconnect conductive structure that is part of the eighth electrical connection has a respective lengthwise centerline oriented along its respective top surface to extend from its corresponding first end to its corresponding second end, with each of the corresponding first edge and the corresponding second edge being substantially straight and oriented substantially parallel to its respective lengthwise centerline.

**21**. The semiconductor chip as recited in claim **14**, wherein two of the first, second, third, fourth, and fifth conductive structures have different lengths.

**22**. The semiconductor chip as recited in claim **21**, wherein the region includes a first connection forming conductive structure positioned to physically join to the top surface of the second conductive structure,

wherein the region includes a second connection forming conductive structure positioned to physically join to the top surface of the third conductive structure,

wherein the region includes a third connection forming conductive structure positioned to physically join to the top surface of the fourth conductive structure,

wherein the region includes a fourth connection forming conductive structure positioned to physically join to the top surface of the fifth conductive structure,

wherein at least one of the first, second, third, and fourth connection forming conductive structures is positioned at a respective location that is not directly above any gate electrode of any transistor of the first collection of transistors and that is not directly above any gate electrode of any transistor of the second collection of transistors and that is not directly above the inner sub-region of the region.

**23**. The semiconductor chip as recited in claim **22**, wherein the first connection forming conductive structure is positioned a first connection distance away from a nearest gate electrode forming portion of the second conductive structure, the first connection distance measured in the first direction between closest located portions of the first connection forming conductive structure and the nearest gate electrode forming portion of the second conductive structure,

wherein the second connection forming conductive structure is positioned a second connection distance away from a nearest gate electrode forming portion of the third conductive structure, the second connection distance measured in the first direction between closest located portions of the second connection forming conductive structure and the nearest gate electrode forming portion of the third conductive structure,

wherein the third connection forming conductive structure is positioned a third connection distance away from a nearest gate electrode forming portion of the fourth conductive structure, the third connection distance measured in the first direction between closest located portions of the third connection forming conductive structure and the nearest gate electrode forming portion of the fourth conductive structure,

wherein the fourth connection forming conductive structure is positioned a fourth connection distance away from a nearest gate electrode forming portion of the fifth conductive structure, the fourth connection distance measured in the first direction between closest located portions of the fourth connection forming conductive structure and the nearest gate electrode forming portion of the fifth conductive structure,

wherein at least two of the first, second, third, and fourth connection distances are different.

**24**. The semiconductor chip as recited in claim **23**, wherein the seventh electrical connection includes one or more overlying interconnect conductive structures formed at a respective vertical position within the semiconductor chip overlying some of the at least eight conductive structures so as to be separated from the co-planar top surfaces of the at least eight conductive structures by at least one dielectric material,

wherein each overlying interconnect conductive structure that is part of the seventh electrical connection has a respective top surface with an entirety of a periphery of the respective top surface defined by a corresponding first end, a corresponding second end, a corresponding first edge, and a corresponding second edge, such that a total distance along the entirety of the periphery of the respective top surface is equal to a sum of a total distance along the corresponding first edge and a total distance along the corresponding second edge and a total distance along the corresponding first end and a total distance along the corresponding second end,

wherein the total distance along the corresponding first edge is greater than two times the total distance along the corresponding first end and is greater than two times the total distance along the corresponding second end, wherein the total distance along the corresponding second edge is greater than two times the total distance along the corresponding first end and is greater than two times the total distance along the corresponding second end,

wherein the corresponding first end extends from the corresponding first edge to the corresponding second edge and is located principally within a space between the corresponding first edge and the corresponding second edge, wherein the corresponding second end extends from the corresponding first edge to the corresponding second edge and is located principally within a space between the corresponding first edge and the corresponding second edge,

wherein each overlying interconnect conductive structure that is part of the seventh electrical connection has a respective lengthwise centerline oriented along its respective top surface to extend from its corresponding first end to its corresponding second end, with each of the corresponding first edge and the corresponding second edge being substantially straight and oriented substantially parallel to its respective lengthwise centerline.

**25**. The semiconductor chip as recited in claim **22**, wherein at least two of the first, second, third, and fourth connection forming conductive structures is positioned at a respective location that is not directly above any gate electrode of any transistor of the first collection of transistors and that is not directly above any gate electrode of any transistor of the second collection of transistors and that is not directly above the inner sub-region of the region.

**26**. The semiconductor chip as recited in claim **25**, wherein at least one of the at least eight conductive structures within the region is a non-gate forming conductive structure that does not form a gate electrode of any transistor,

the non-gate forming conductive structure positioned between at least two neighboring conductive structures of the at least eight conductive structures, with at least

one of the at least two neighboring conductive structures forming at least one gate electrode of at least one transistor,

the non-gate forming conductive structure positioned such that its lengthwise centerline is separated from the lengthwise centerlines of each of the at least two neighboring conductive structures by the first pitch as measured in the second direction,

the non-gate forming conductive structure having a width as measured in the second direction that is substantially equal to a width as measured in the second direction of at least one of the at least two neighboring conductive structures.

**27**. The semiconductor chip as recited in claim **26**, wherein the region includes a first gate contact positioned to physically contact the top surface of the first conductive structure, the first gate contact substantially centered in the second direction upon the first conductive structure, the first gate contact formed to extend in a vertical direction substantially perpendicular to the substrate of the semiconductor chip from the top surface of the first conductive structure through a dielectric material to contact at least one interconnect conductive structure,

wherein the region includes a second gate contact positioned to physically contact the top surface of the second conductive structure, the second gate contact substantially centered in the second direction upon the second conductive structure, the second gate contact formed to extend in the vertical direction substantially perpendicular to the substrate of the semiconductor chip from the top surface of the second conductive structure through the dielectric material to contact at least one interconnect conductive structure,

wherein the region includes a third gate contact positioned to physically contact the top surface of the third conductive structure, the third gate contact substantially centered in the second direction upon the third conductive structure, the third gate contact formed to extend in the vertical direction substantially perpendicular to the substrate of the semiconductor chip from the top surface of the third conductive structure through the dielectric material to contact at least one interconnect conductive structure,

wherein the region includes a fourth gate contact positioned to physically contact the top surface of the fourth conductive structure, the fourth gate contact substantially centered in the second direction upon the fourth conductive structure, the fourth gate contact formed to extend in the vertical direction substantially perpendicular to the substrate of the semiconductor chip from the top surface of the fourth conductive structure through the dielectric material to contact at least one interconnect conductive structure,

wherein the region includes a fifth gate contact positioned to physically contact the top surface of the fifth conductive structure, the fifth gate contact substantially centered in the second direction upon the fifth conductive structure, the fifth gate contact formed to extend in the vertical direction substantially perpendicular to the substrate of the semiconductor chip from the top surface of the fifth conductive structure through the dielectric material to contact at least one interconnect conductive structure.

**28**. The semiconductor chip as recited in claim **26**, wherein the seventh electrical connection includes one or more overlying interconnect conductive structures formed at a respective vertical position within the semiconductor chip overlying some of the at least eight conductive structures so as to be separated from the co-planar top surfaces of the at least eight conductive structures by at least one dielectric material,

wherein each overlying interconnect conductive structure that is part of the seventh electrical connection has a respective top surface with an entirety of a periphery of the respective top surface defined by a corresponding first end, a corresponding second end, a corresponding first edge, and a corresponding second edge, such that a total distance along the entirety of the periphery of the respective top surface is equal to a sum of a total distance along the corresponding first edge and a total distance along the corresponding second edge and a total distance along the corresponding first end and a total distance along the corresponding second end,

wherein the total distance along the corresponding first edge is greater than two times the total distance along the corresponding first end and is greater than two times the total distance along the corresponding second end, wherein the total distance along the corresponding second edge is greater than two times the total distance along the corresponding first end and is greater than two times the total distance along the corresponding second end,

wherein the corresponding first end extends from the corresponding first edge to the corresponding second edge and is located principally within a space between the corresponding first edge and the corresponding second edge, wherein the corresponding second end extends from the corresponding first edge to the corresponding second edge and is located principally within a space between the corresponding first edge and the corresponding second edge,

wherein each overlying interconnect conductive structure that is part of the seventh electrical connection has a respective lengthwise centerline oriented along its respective top surface to extend from its corresponding first end to its corresponding second end, with each of the corresponding first edge and the corresponding second edge being substantially straight and oriented substantially parallel to its respective lengthwise centerline.

**29**. A method for manufacturing an integrated circuit within a semiconductor chip, comprising:

forming a plurality of transistors within a region of the semiconductor chip, each of the plurality of transistors in the region forming part of circuitry associated with execution of one or more logic functions, the plurality of transistors having respective gate electrodes formed by some of at least eight conductive structures present within the region,

wherein forming the plurality of transistors includes forming each of the at least eight conductive structures to respectively have a corresponding top surface, wherein an entirety of a periphery of the corresponding top surface is defined by a corresponding first end, a corresponding second end, a corresponding first edge, and a corresponding second edge, such that a total distance along the entirety of the periphery of the corresponding top surface is equal to a sum of a total distance along the corresponding first edge and a total distance along the corresponding second edge and a total distance along the corresponding first end and a total distance along the corresponding second end,

wherein the total distance along the corresponding first edge is greater than two times the total distance along the corresponding first end,

wherein the total distance along the corresponding first edge is greater than two times the total distance along the corresponding second end,

wherein the total distance along the corresponding second edge is greater than two times the total distance along the corresponding first end,

wherein the total distance along the corresponding second edge is greater than two times the total distance along the corresponding second end,

wherein the corresponding first end extends from the corresponding first edge to the corresponding second edge and is located principally within a space between the corresponding first and second edges,

wherein the corresponding second end extends from the corresponding first edge to the corresponding second edge and is located principally within the space between the corresponding first and second edges,

the top surfaces of the at least eight conductive structures co-planar with each other,

wherein forming the plurality of transistors includes forming each of the at least eight conductive structures to have a corresponding lengthwise centerline oriented in a first direction along its top surface and extending from its first end to its second end,

each of the at least eight conductive structures having a length as measured along its lengthwise centerline from its first end to its second end,

wherein the first edge of each of the at least eight conductive structures is substantially straight,

wherein the second edge of each of the at least eight conductive structures is substantially straight,

each of the at least eight conductive structures having both its first edge and its second edge oriented substantially parallel to its lengthwise centerline,

each of the at least eight conductive structures having a width measured in a second direction perpendicular to the first direction at a midpoint of its lengthwise centerline, wherein the width of each of the at least eight conductive structures is less than 45 nanometers,

each of the first direction and the second direction oriented substantially parallel to the co-planar top surfaces of the at least eight conductive structures,

wherein forming the plurality of transistors includes positioning the at least eight conductive structures in a side-by-side manner such that each of the at least eight conductive structures is positioned to have at least a portion of its length beside at least a portion of the length of another of the at least eight conductive structures,

and wherein each of the at least eight conductive structures is positioned such that a distance as measured in the second direction between its lengthwise centerline and the lengthwise centerline of at least one other of the at least eight conductive structures is substantially equal to a first pitch that is less than or equal to about 193 nanometers,

the at least eight conductive structures including a first conductive structure, the first conductive structure including a portion that forms a gate electrode of first transistor of a first transistor type, the first conductive structure including a portion that forms a gate electrode of a first transistor of a second transistor type,

the at least eight conductive structures including a second conductive structure, the second conductive structure including a portion that forms a gate electrode of a second transistor of the first transistor type, wherein any transistor having its gate electrode formed by the second conductive structure is of the first transistor type,

the at least eight conductive structures including a third conductive structure, the third conductive structure including a portion that forms a gate electrode of a second transistor of the second transistor type, wherein any transistor having its gate electrode formed by the third conductive structure is of the second transistor type,

the at least eight conductive structures including a fourth conductive structure, the fourth conductive structure including a portion that forms a gate electrode of a third transistor of the first transistor type, wherein any transistor having its gate electrode formed by the fourth conductive structure is of the first transistor type,

the at least eight conductive structures including a fifth conductive structure, the fifth conductive structure including a portion that forms a gate electrode of a third transistor of the second transistor type, wherein any transistor having its gate electrode formed by the fifth conductive structure is of the second transistor type,

the first transistor of the first transistor type including a first diffusion terminal electrically connected to a first diffusion terminal of the second transistor of the first transistor type through a first electrical connection,

the first transistor of the second transistor type including a first diffusion terminal electrically connected to a first diffusion terminal of the second transistor of the second transistor type through a second electrical connection,

the second transistor of the first transistor type including a second diffusion terminal electrically connected to a first diffusion terminal of the third transistor of the first transistor type through a third electrical connection,

the second transistor of the second transistor type including a second diffusion terminal electrically connected to a first diffusion terminal of the third transistor of the second transistor type through a fourth electrical connection,

the third transistor of the first transistor type including a second diffusion terminal electrically connected to a first diffusion terminal of a fourth transistor of the first transistor type through a fifth electrical connection,

the third transistor of the second transistor type including a second diffusion terminal electrically connected to a first diffusion terminal of a fourth transistor of the second transistor type through a sixth electrical connection,

wherein the third electrical connection is electrically connected to the fourth electrical connection through a seventh electrical connection,

wherein the gate electrode of the second transistor of the first transistor type is electrically connected to the gate electrode of the third transistor of the second transistor type through an eighth electrical connection,

wherein the gate electrode of the third transistor of the first transistor type is electrically connected to the gate electrode of the second transistor of the second transistor type through a ninth electrical connection,

wherein each transistor of the first transistor type having its gate electrode formed by any of the at least eight conductive structures is included in a first collection of transistors, and wherein each transistor of the second transistor type having its gate electrode formed by any of the at least eight conductive structures is included in a second collection of transistors, wherein the first collection of transistors is separated from the second collection of transistors by an inner sub-region of the region, wherein the inner sub-region does not include a source or a drain of any transistor,

wherein the region has a size of about 965 nanometers as measured in the second direction.

**30**. The method as recited in claim **29**, further comprising:

forming a first interconnect conductive structure within the region at a position within either of a first interconnect level, a second interconnect level, a third interconnect level, or a fourth interconnect level,

the first interconnect conductive structure formed to have a top surface, an entirety of a periphery of the top surface of the first interconnect conductive structure defined by a first end of the first interconnect conductive structure, a second end of the first interconnect conductive structure, a first edge of the first interconnect conductive structure, and a second edge of the first interconnect conductive structure, such that a total distance along the entirety of the periphery of the top surface of the first interconnect conductive structure is equal to a sum of a total distance along the first edge of the first interconnect conductive structure and a total distance along the second edge of the first interconnect conductive structure and a total distance along the first end of the first interconnect conductive structure and a total distance along the second end of the first interconnect conductive structure,

wherein the total distance along the first edge of the first interconnect conductive structure is greater than two times the total distance along the first end of the first interconnect conductive structure,

wherein the total distance along the first edge of the first interconnect conductive structure is greater than two times the total distance along the second end of the first interconnect conductive structure,

wherein the total distance along the second edge of the first interconnect conductive structure is greater than two times the total distance along the first end of the first interconnect conductive structure,

wherein the total distance along the second edge of the first interconnect conductive structure is greater than two times the total distance along the second end of the first interconnect conductive structure,

wherein the first end of the first interconnect conductive structure extends from the first edge of the first interconnect conductive structure to the second edge of the first interconnect conductive structure and is located principally within a space between the first and second edges of the first interconnect conductive structure,

wherein the second end of the first interconnect conductive structure extends from the first edge of the first interconnect conductive structure to the second edge of the first interconnect conductive structure and is located principally within the space between the first and second edges of the first interconnect conductive structure,

the first interconnect conductive structure having a lengthwise centerline oriented in the second direction along its top surface and extending from its first end to its second end,

wherein the first edge of the first interconnect conductive structure is substantially straight and is oriented substantially parallel to the lengthwise centerline of the first interconnect conductive structure,

wherein the second edge of the first interconnect conductive structure is substantially straight and is oriented substantially parallel to the lengthwise centerline of the first interconnect conductive structure,

wherein the first interconnect conductive structure has a length measured along its lengthwise centerline from its first end to its second end,

wherein the first interconnect conductive structure has a width measured in the first direction perpendicular to the second direction at a midpoint of the lengthwise centerline of the first interconnect conductive structure,

wherein the first interconnect level is located at a vertical position within the semiconductor chip above the at least eight conductive structures, wherein the first interconnect level is separated from the co-planar top surfaces of the at least eight conductive structures by at least one dielectric material,

wherein the second interconnect level is located at a vertical position within the semiconductor chip above the first interconnect level,

wherein the third interconnect level is located at a vertical position within the semiconductor chip above the second interconnect level,

wherein the fourth interconnect level is located at a vertical position within the semiconductor chip above the third interconnect level;

forming a second interconnect conductive structure within the region at a position in a same interconnect level as the first interconnect conductive structure,

the second interconnect conductive structure formed to have a top surface, an entirety of a periphery of the top surface of the second interconnect conductive structure defined by a first end of the second interconnect conductive structure, a second end of the second interconnect conductive structure, a first edge of the second interconnect conductive structure, and a second edge of the second interconnect conductive structure, such that a total distance along the entirety of the periphery of the top surface of the second interconnect conductive structure is equal to a sum of a total distance along the first edge of the second interconnect conductive structure and a total distance along the second edge of the second interconnect conductive structure and a total distance along the first end of the second interconnect conductive structure and a total distance along the second end of the second interconnect conductive structure,

wherein the total distance along the first edge of the second interconnect conductive structure is greater than two times the total distance along the first end of the second interconnect conductive structure,

wherein the total distance along the first edge of the second interconnect conductive structure is greater than two times the total distance along the second end of the second interconnect conductive structure,

wherein the total distance along the second edge of the second interconnect conductive structure is greater than two times the total distance along the first end of the second interconnect conductive structure,

wherein the total distance along the second edge of the second interconnect conductive structure is greater than two times the total distance along the second end of the second interconnect conductive structure,

wherein the first end of the second interconnect conductive structure extends from the first edge of the second interconnect conductive structure to the second edge of the second interconnect conductive structure and is located principally within a space between the first and second edges of the second interconnect conductive structure,

wherein the second end of the second interconnect conductive structure extends from the first edge of the second interconnect conductive structure to the second edge of the second interconnect conductive structure and is

located principally within the space between the first and second edges of the second interconnect conductive structure,

the second interconnect conductive structure having a lengthwise centerline oriented in the second direction along its top surface and extending from its first end to its second end,

wherein the first edge of the second interconnect conductive structure is substantially straight and is oriented substantially parallel to the lengthwise centerline of the second interconnect conductive structure,

wherein the second edge of the second interconnect conductive structure is substantially straight and is oriented substantially parallel to the lengthwise centerline of the second interconnect conductive structure,

wherein the second interconnect conductive structure has a length measured along its lengthwise centerline from its first end to its second end,

wherein the second interconnect conductive structure has a width measured in the first direction perpendicular to the second direction at a midpoint of the lengthwise centerline of the second interconnect conductive structure,

wherein the first and second interconnect conductive structures are positioned next to and spaced apart from each other such that a distance as measured in the first direction between their lengthwise centerlines is substantially equal to a second pitch;

forming a third interconnect conductive structure within the region at a position in the same interconnect level as the first and second interconnect conductive structures,

the third interconnect conductive structure formed to have a top surface, an entirety of a periphery of the top surface of the third interconnect conductive structure defined by a first end of the third interconnect conductive structure, a second end of the third interconnect conductive structure, a first edge of the third interconnect conductive structure, and a second edge of the third interconnect conductive structure, such that a total distance along the entirety of the periphery of the top surface of the third interconnect conductive structure is equal to a sum of a total distance along the first edge of the third interconnect conductive structure and a total distance along the second edge of the third interconnect conductive structure and a total distance along the first end of the third interconnect conductive structure and a total distance along the second end of the third interconnect conductive structure,

wherein the total distance along the first edge of the third interconnect conductive structure is greater than two times the total distance along the first end of the third interconnect conductive structure,

wherein the total distance along the first edge of the third interconnect conductive structure is greater than two times the total distance along the second end of the third interconnect conductive structure,

wherein the total distance along the second edge of the third interconnect conductive structure is greater than two times the total distance along the first end of the third interconnect conductive structure,

wherein the total distance along the second edge of the third interconnect conductive structure is greater than two times the total distance along the second end of the third interconnect conductive structure,

wherein the first end of the third interconnect conductive structure extends from the first edge of the third interconnect conductive structure to the second edge of the third interconnect conductive structure and is located principally within a space between the first and second edges of the third interconnect conductive structure,

wherein the second end of the third interconnect conductive structure extends from the first edge of the third interconnect conductive structure to the second edge of the third interconnect conductive structure and is located principally within the space between the first and second edges of the third interconnect conductive structure,

the third interconnect conductive structure having a lengthwise centerline oriented in the second direction along its top surface and extending from its first end to its second end,

wherein the first edge of the third interconnect conductive structure is substantially straight and is oriented substantially parallel to the lengthwise centerline of the third interconnect conductive structure,

wherein the second edge of the third interconnect conductive structure is substantially straight and is oriented substantially parallel to the lengthwise centerline of the third interconnect conductive structure,

wherein the third interconnect conductive structure has a length measured along its lengthwise centerline from its first end to its second end,

wherein the third interconnect conductive structure has a width measured in the first direction perpendicular to the second direction at a midpoint of the lengthwise centerline of the third interconnect conductive structure; and

forming a fourth interconnect conductive structure within the region at a position in the same interconnect level as the first, second, and third interconnect conductive structures,

the fourth interconnect conductive structure formed to have a top surface, an entirety of a periphery of the top surface of the fourth interconnect conductive structure defined by a first end of the fourth interconnect conductive structure, a second end of the fourth interconnect conductive structure, a first edge of the fourth interconnect conductive structure, and a second edge of the fourth interconnect conductive structure, such that a total distance along the entirety of the periphery of the top surface of the fourth interconnect conductive structure is equal to a sum of a total distance along the first edge of the fourth interconnect conductive structure and a total distance along the second edge of the fourth interconnect conductive structure and a total distance along the first end of the fourth interconnect conductive structure and a total distance along the second end of the fourth interconnect conductive structure,

wherein the total distance along the first edge of the fourth interconnect conductive structure is greater than two times the total distance along the first end of the fourth interconnect conductive structure,

wherein the total distance along the first edge of the fourth interconnect conductive structure is greater than two times the total distance along the second end of the fourth interconnect conductive structure,

wherein the total distance along the second edge of the fourth interconnect conductive structure is greater than two times the total distance along the first end of the fourth interconnect conductive structure,

wherein the total distance along the second edge of the fourth interconnect conductive structure is greater than two times the total distance along the second end of the fourth interconnect conductive structure,

wherein the first end of the fourth interconnect conductive structure extends from the first edge of the fourth interconnect conductive structure to the second edge of the

fourth interconnect conductive structure and is located principally within a space between the first and second edges of the fourth interconnect conductive structure,

wherein the second end of the fourth interconnect conductive structure extends from the first edge of the fourth interconnect conductive structure to the second edge of the fourth interconnect conductive structure and is located principally within the space between the first and second edges of the fourth interconnect conductive structure,

the fourth interconnect conductive structure having a lengthwise centerline oriented in the second direction along its top surface and extending from its first end to its second end,

wherein the first edge of the fourth interconnect conductive structure is substantially straight and is oriented substantially parallel to the lengthwise centerline of the fourth interconnect conductive structure,

wherein the second edge of the fourth interconnect conductive structure is substantially straight and is oriented substantially parallel to the lengthwise centerline of the fourth interconnect conductive structure,

wherein the fourth interconnect conductive structure has a length measured along its lengthwise centerline from its first end to its second end,

wherein the fourth interconnect conductive structure has a width measured in the first direction perpendicular to the second direction at a midpoint of the lengthwise centerline of the fourth interconnect conductive structure,

wherein the third and fourth interconnect conductive structures are positioned next to and spaced apart from each other such that a distance as measured in the first direction between their lengthwise centerlines is substantially equal to the second pitch.

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